Built-In-Self-Test systems for Analog Mixed-Signal system LSI

Project Leader

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Faculty Members involved in this Project

None

Objective

Develop Built-In-Self-Test (BIST) systems for Analog-Mixed-Signal (AMS) system LSI. This system consists of small analog circuit to observe various circuit nodes of analog system (observer circuits) and logic circuits control observer circuits and decide analog circuits have defect or not. Main objectives of this research project are (i) develop observer circuits and design those as library elements, (ii) develop algorithms and programs to generate logic systems from defined test procedure, (iii) develop interface programs with place-and-route EDA systems for LSI. Also static or dynamic analyzing method or algorithm to find out which node in analog circuits should be observed to detect defect of circuit will be developed.

Project Outline

(1) Review of past investigations

(2) Develop Observer circuits which should have following characteristics, (i) The area needed to realize observer circuits is small enough to built in to AMS LSI, (ii) Power consumptions of observer circuits should be ZERO or negligibly low in system's normal operation, (iii) Observer circuits are designed as library elements.

(3) Define language to describe Test Procedure and develop algorithms and programs to generate logic circuits from described test procedure. The Test Procedure also defines the node points in analog circuit to observe.

(4) Develop interface programs with the existing place-and-route EDA systems for LSI. With other part of AMS system, the observer circuits and control circuits should be designed into LSI pattern by using existing EDA system for LSI.

(5) Develop (static or dynamic) analyzing method (or algorithm) to find out which node points in analog circuits are suitable to Built-In-Self-Test.

References

(1) Wimol San-UM, Masayoshi Tachibana, A Fault Signature Characterization Based Analog Circuit Testing Scheme and the Extension of IEEE 1149.4 Standard", The IEICE Transactions on Information and Systems, Vol.E93-D,No.1,pp33-42,2010

(2) Wimol San-UM, Masayoshi Tachibana," A Low-Cost High-Speed Pulse Response Based Built-In Self Test For Analog Integrated Circuits", ECTI Transaction on Electrical Engineering, Electronics, and Communications, Vol.8,No.2, pp197-208,2010

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