DEVELOPMENT DESIGN OF BUILT-IN SELF-TEST FOR LSI CIRCUITS: TEST PATTERN GENERATION, OSCILLATION-BASED TESTING, AND CALIBRATION TECHNIQUE

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1198007 Chatchai Wannaboon

Advisor Prof. Masayoshi Tachibana

Electronic and Photonic Systems Engineering Course
Graduate School of Engineering, Kochi University of Technology

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The title of this dissertation on September 5, 2018 was “DEVELOPMENT DESIGN OF BUILT-IN SELF-TEST FOR LSI CIRCUITS: TEST PATTERN GENERATOR, OSCILLATIONBASED TESTING, AND CALIBRATION TECHNIQUE,” and it was modified on September 20, 2018.

Abstract

There are three major activities in the life-cycle of an ICs product, i.e. design, manufacturing, and testing. A robust design and proper manufacturing environment provide a quality performance of the devices. Besides, testing is required to improve a reliability of the manufactured ICs. Despite outstanding design and fabrication process, it is futile to achieve a complete quality ICs without a suitable testing strategy. Typically, testing is required in every phases in the life-cycle of the ICs product. In other words, testing, in terms of design verification, identifies numerical errors during the design phase. Likewise, during the fabrication process, testing prevents any manufactured defects and ensure the quality of the designed product. Testing also seeks to detect functional faults that sustained during operation.

Rising of the transistor technology has evolved the electronic industry substantially. From the visible with normal size, nowadays, modern electronics device is implemented and operated on a Nano-scale and tends to reducing every year. Meanwhile, the size of electronics device is decreasing, the quality is approaching to the opposite direction. In other words, the quantity and diversity of transistors is increasing, and become a high complex network. This situation has led to a great demand of reliable System on Chip (SoC). Testing such devices before a manufacturing process has become a crucial issue. Although, an off-chip testing with automated test equipment has been used commercially, it requires costly measurements with long-time process. For contemporary Large Scale Integrated (LSI) circuits, automated on-chip testing has gained a great attention on either research or industrial area. Built-in Self-Test (BIST) and Design-for-Test (DFT) are the major strategies, which have been widely accepted by meaning of improving observability and controllability during the testing process.

This dissertation presents effective designs of BIST systems for a defect-oriented testing in analog and mixed-signals LSI circuits. Fully on-chip circuitry, high faults detection against catastrophic and parametric variation, and low performance degradation are the objectives of this work. The proposed methods focus on the principal of BIST, i.e. test stimulus generation, test control, and test response analysis. Such methods are implemented for essential LSI building blocks, ranging from transistor-only circuitry such as an operational amplifier (Op Amp) and comparator, to an analog low-pass filter, as well as a large-scale mixed-signals system. The major contributions of this dissertation can be classified into three approaches. The first approach is designing a high-speed random signals generator for the source of test stimulus generation. The second approach is the demonstration of an oscillation-based testing in order to eliminate the large stimulus generator. The third approach involves the combination of self-test and calibration technique for each circuit elements.

The proposed methods of this dissertation begins with a high-data-rate true random bit generator for a cost-effective and high-speed test stimulus generation. This method is a full-custom design of chaos-based True Random-Bit Generator (TRBG) implemented on a 0.18-μm CMOS technology with unique composition of three major components, i.e. (i) chaotic jerk oscillator, (ii) $\Delta\Sigma$ modulator, and (iii) simple pre/post-processing. A chaotic jerk oscillator is a deterministic source of randomness that potentially offers robust and highly random chaotic signals and exhibits a distinctive property of smoothly balanced-to-unbalanced alternation of double-scroll attractors. The continuous-time 2^{nd}-order $\Delta\Sigma$ modulator is introduced as a mixed-signal interface in order to increase a resolution of random bit sequences while no extra clock is required. The $\Delta\Sigma$ modulator is constructed mainly by a folded-cascode amplifier with sufficient gain and phase margin of 64dB and 83°, respectively, and a high-speed comparator with a time constant of 2.7ns. An uncomplicated structure of shift-registers is realized as a post-processing

process. The bit sequence of the proposed TRBG successfully passes all statistical tests of NIST SP800-22 test suite, and the ultimate output bit rate is 50Mbps. The physical layout of a chip area is 212.8 × 177.11 μm^2 and the DC power dissipation is 1.32mW using a 1.8-V single supply voltage.

The second method, a simple design-for-testability (DFT) technique for analog second-order $\Delta\Sigma$ modulators is described. The structure of circuit-under-test is modified and operated as two symmetric structure circuits in the test mode. Different DC offset and simple digital counters are connected to the input and output of the circuit in order to reduce testing process complications and costs, with the modulator operated as a simple signal generator in the test mode. A demonstration of the testing process is performed through the switched-capacitor second-order $\Delta\Sigma$ modulator, which achieves several advantages, including low cost, high-speed testing, and high fault coverage, and covers parametric failure. Also, the overall system was fully fabricated in 0.18-μm CMOS standard technology without the need for additional digital processing units.

Additionally, a phase difference analysis technique is presented in the third method, which is sensitive to the parametric deviations and allows a tolerance band of passive analog components. Test operations can be simply achieved by comparing the phase difference between a reference clock signal and a reconfigured circuit-under-test (CUT) as an oscillator. The difference of phase characteristics between the two signals can be utilized as an indicator for a fault signature, which can be characterized by a compact digital circuit comprising a counter and logic components. Simulation of faults detection reveals a high faults coverage, high-speed testing, and tolerance band controllability. The proposed technique has offered a fully on-chip BIST in 0.18-μm CMOS standard technology with no external test equipment required.

Furthermore, the integration of BIST and calibration technique is proposed in the forth method. simple circuitry such as a frequency-to-DC circuit, a windows compara-

tor, and basic logic elements are utilized as the faults detection circuits. The calibration system is additionally implemented through the resistor array with a feedback network in order to adjust the gain value of the CUT. Simulation results show the capable of faults detection involves catastrophic and parametric variation. Moreover, the signals-to-noise ratio (SNR) of the CUT can be preserved at the acceptable level against the failure circuitry.

key words Built-In Self-Test, Test and Calibration Technique, Oscillation-Based Testing, True Random Bit Generation, Chaotic Oscillator, Design-for-Structural-Testability.

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Chapter 1

Introduction

The demand of microelectronics devices has been growing doubly over the past two decades, due to the variety features of complementary metal oxide semiconductor (CMOS) process, i.e. low power, integration capability, and inexpensive manufacturing process. As a result, electronics industry has attempted to produces the devices at substantially lower cost per function with higher performance year after year. Scaling down the transistor size is the key factor of this issue. Otherwise, all dimensions of a CMOS transistor are scaled while preserving its behavior, yielding to larger amount of transistors and higher complexity integrated circuits (ICs). Every reduction of transistor size, cheaper and higher speeds of micro-processors are enabled. These developments lead to the evolution in numerous application domains such as communications, industry, and computer technology.

It is apparent that scaling down the transistors size into deeper sub-micron trends to proceed continuously. Likewise, the difficulty of design and manufacture has concurrently increased where the designing of perfect ICs seem to reach the unrealistic. For example, scaling a junction depths and gate oxide thickness may sustain the large variation of CMOS transistor parameters, resulting in unusual delays and leakage currents. These phenomenon occurs when more transistors are densely fabricated per unit area. In other words, number of transistors and wire have become larger, creating a larger area to sustain manufacturing defects. The transistor sizes have become smaller, increasing the volume and variety of defects during the fabrication process. Consequently, small

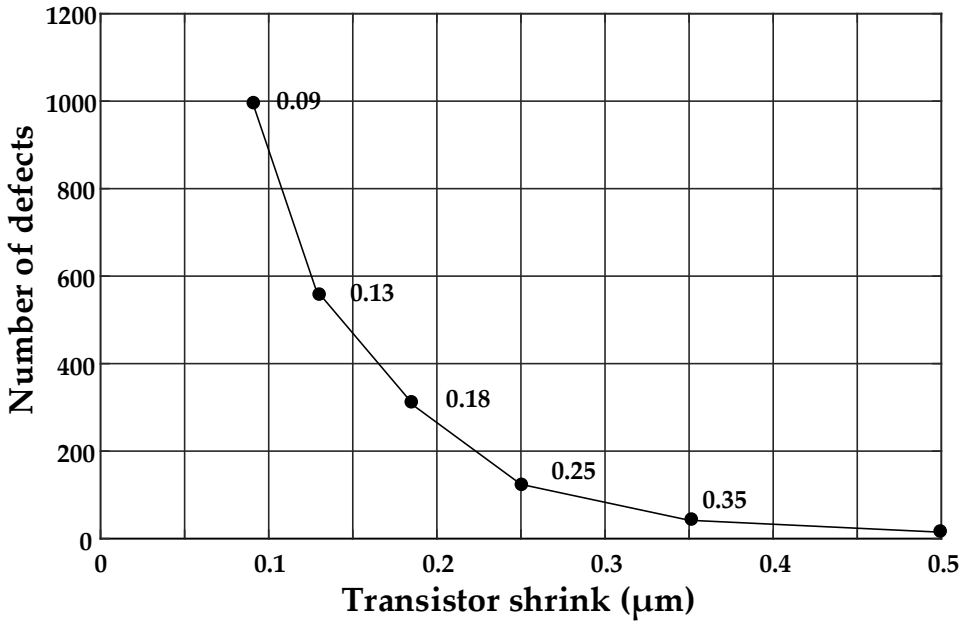

Fig. 1.1 Number of defects versus transistor shrinking size.

defects and imperfections are created during the manufacturing process and cause the failure circuits. Fig. 1.1 shows the number of defects during the manufacturing process versus transistor shrinking size. It can be clearly seen that deeper sub-micron technology causes higher number of defects in an exponential behavior. This issue necessitate the requirement of reliable ICs. Testing has become an important part to improve the quality and reliability of manufacturing ICs process, which has widely gained an attention on either research and industrial area.

This chapter introduce the necessary issue, beginning with the necessary of testing in an integrated circuit design. Underlying of defects in the realistic ICs production is lately described. Afterward, classification of testing architectures are briefly presented. The objective and organization of this dissertation are also described in the end of chapter.

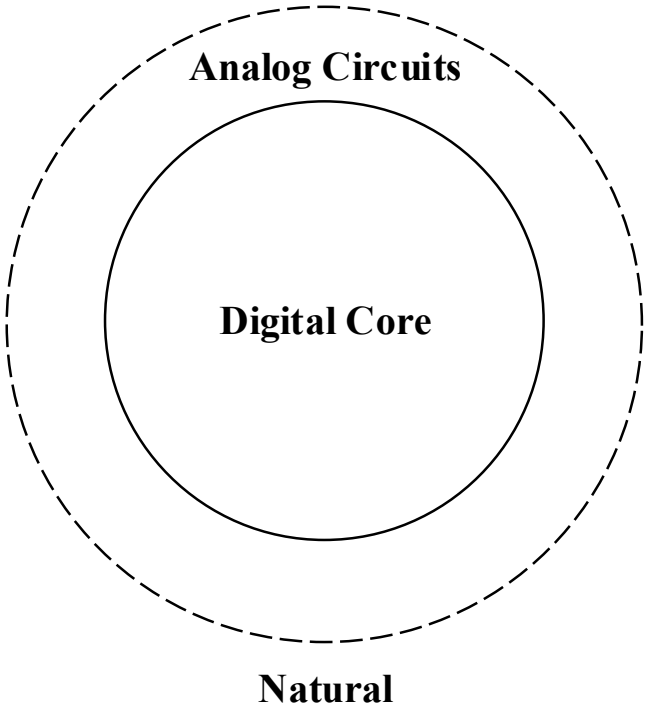

Fig. 1.2 The role of analog circuits in overall electronically process.

1.1 An overview of Mixed-Signal Testing

Sound, temperature, light density and velocity are dynamically quantities. Such a natural phenomenon is continuously varying in terms of magnitude and time. Processing these information from environment needs the advantages of an analog and digital system. The role of analog circuits is dealing with the input signals directly such as amplifying, filtering and converting. While digital circuits operate the analog signals logically at discrete intervals and generate the result values. The output of the system may be converted back to the natural signals by analog circuits at the end of process. Fig. 1.2 depicts the role of analog circuits in overall electronically process. The analog circuit is the interface between natural information and digital system which may be defined as a pre/post-processing part in the electronically process. This integration of analog and digital system in single device is called mixed-signal system, which is widely

used in modern applications.

Testing in the mixed-signal system is often operated in the individual part, i.e. analog and digital. In digital circuits, the input and output signals are realized in terms of logical (Boolean) and the performance is controllable depending on a programming language constructs. Test strategy can be simply designed by storing the binary distinction patterns in the memory. Unlike digital systems, analog systems are mainly nonlinear and their performance is determined by circuit parameters. Such behavior is complex and difficult to design the pass/fail conditions in terms of logical. Analog circuits also heavily suffer from process variation which can cause unacceptable performance degradation. Therefore, analog circuits is further susceptible to defects owing to the time and voltage continuous nature of their operation. Test complexity is the main issue of analog circuits where the proper test strategy are needed to discriminate between various pattern of faulty conditions and the fail-free condition.

1.2 Defects in the Integrated Circuits

Defects can be classified into two categories, i.e. local and global. The local defects randomly occur within an IC, while the global defects distribute and affect in complete region of a wafer. This research deal with the local defects, which regularly caused by tiny dust, imperfection of fabrication process, etc. Some defects arise from process variability such as implantation and diffusion process. Fig. 1.3 illustrates a sample of defect types during the manufacturing process. The effect of defects on the circuit performance depends on a size and area of distribution. In other words, a single large particle may cause a short or open faulty circuitry, while a vast distribution of tiny particle may unaffected apparently. However its may cause a deviation in specifications, e.g. delay, gain error, current leakage, etc. Hence, the faults in ICs can be classified as

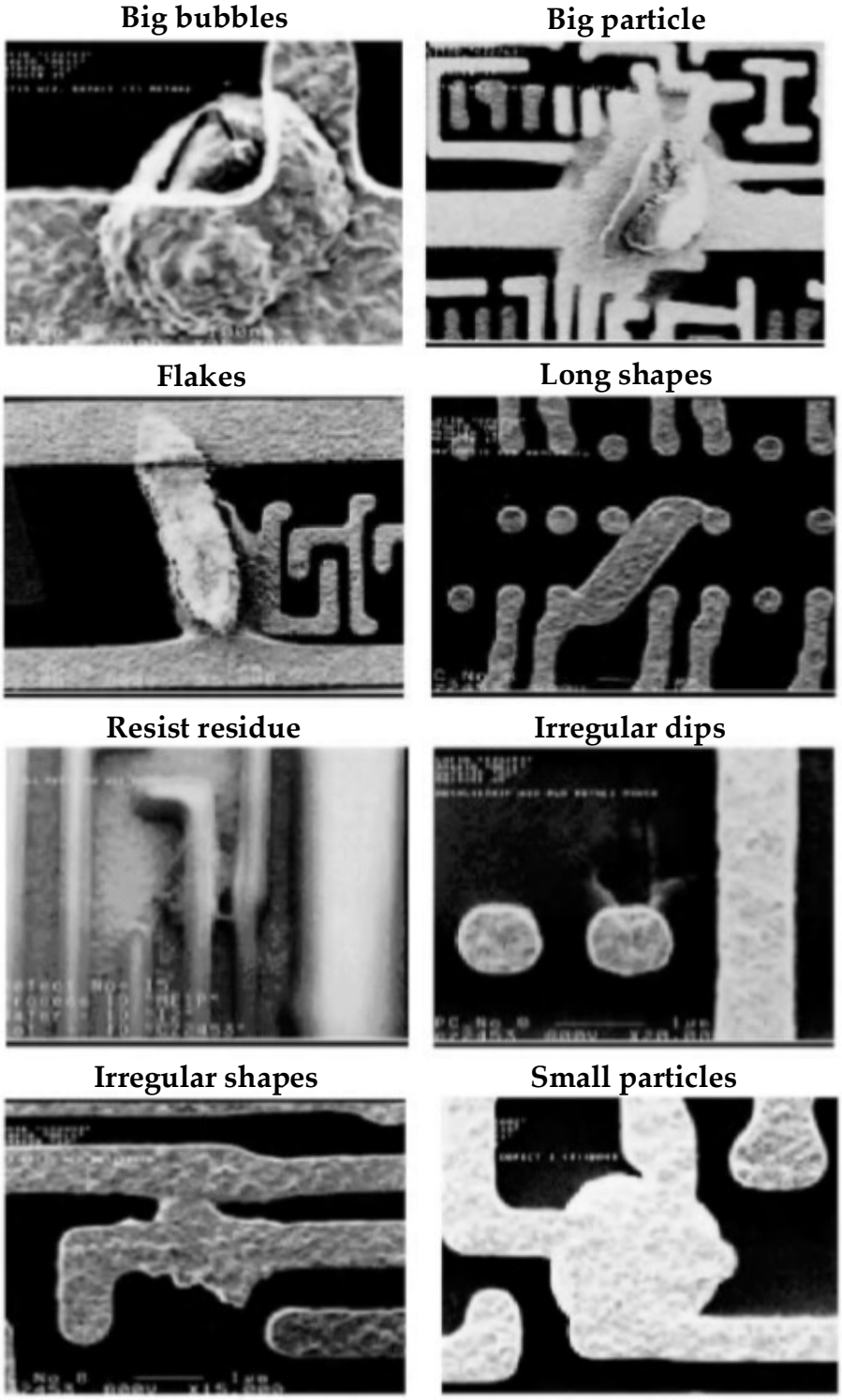

Fig. 1.3 Sample of defects in manufactured ICs.

a catastrophic or parametric. The catastrophic or hard faults are occurred by random large defects during the implantation or diffusion process causing an open, short, extra

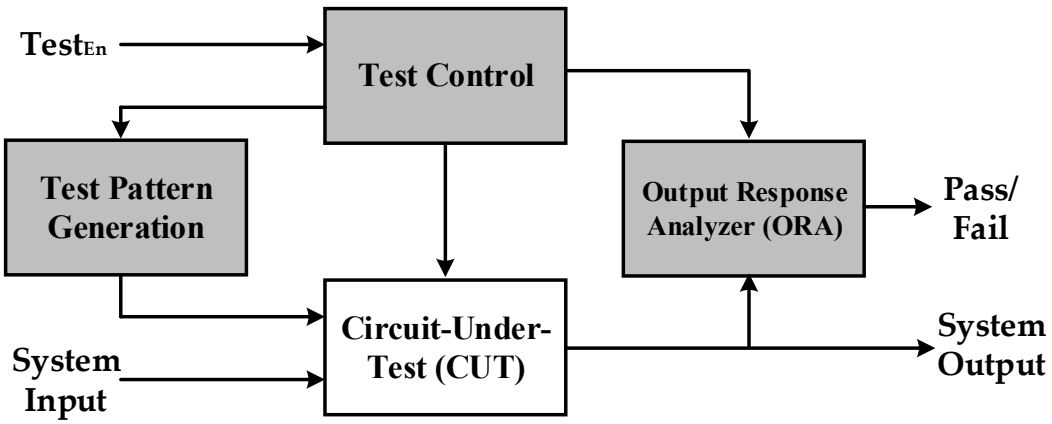

Fig. 1.4 Basic BIST architecture.

device and missing functional behavior of the IC. On the other hand, the parametric or soft faults are due to small defects that too minor to cause hard faults, which slightly deviates the circuit parameter from their designed value.

The parametric faults is a crucial issue in the ICs testing process, due to unpredictable and practically undetectable with the ordinary testing methods. In addition, modeling of parametric faults seem to be an unrealistic, especially in analog circuits. Detection of this fault requires a complex algorithm and high accuracy measurements, which directly impact to the testing cost. Therefore, modern ICs design is aims to reduce these troubles and become a challenge.

1.3 Brief Classification of Testing Architecture

The integrated circuits are very large variations in property, structure and performances, so specific testing methods are required in each sub-circuit. As mentioned in previous section, faults detection in analog circuits is relatively difficult because no accepted analog fault model exists. However, almost system-on-chips (SOC) contain not only the analog circuit but also digital portions such as analog-to-digital converter (ADCs), digital-to-analog converters (DACs), phase-locked-loops circuits, etc. Such cir-

cuits are defined as a mixed-signal circuit. There are many techniques for mixed-signal testing depending on specialized approaches which is integration of digital testing stimulus and parametric measurements. Two major issue for mixed-signal testing are (1) fully on-chip digital/analog test instruments and (2) reduce testing cost though an auto-test equipment (ATE). For this reason, built-in self-test (BIST) technique has widely been studied and utilized in modern mixed-signal circuits.

The underlying idea of BIST is to designing a system that can automatically test itself and return a response in term of "good" or "bad" (fault-free or faulty circuit). The general functionalities are a capable of generating test patterns and correctly perform a test response of the CUT. Consequently, specific circuits are required for providing a test function that can determine whether the CUT covered by BIST circuits are working properly or faulty. Fig. 1.4 depicts the architecture of BIST circuitry includes five essential functions. The two major functions comprise the test pattern generator (TPG) and the output response analyzer (ORA), that provides pattern stimulus for testing and indicate the output response of the CUT into type of pass or fault, respectively. The other two additional functions are test controller and input isolation that are necessary to facilitate execution of self-testing feature. The two distinctive features of BIST cover vertical testing ability and high diagnostic resolution. In the other words, it can be used at all levels testing, i.e. wafer and device-level testing, manufacturing testing, as well as system-level testing. When BIST circuits are enabled in the CUT, the output response indicates not only whether the faults exist in that VLSI device, but also identify the position of faulty circuit in some structure. Whereas designing the proper BIST circuits are reasonably a challenge that the CUT is operated without interference from the BIST circuit. Therefore, the two systems must be designed at least, i.e. a BIST and intended system which both systems must synchronously work together.

1.4 Objectives of this Dissertation

The three major keys in the realization of an IC involves design, fabrication and testing. These three steps should be perfectly balanced in order to achieve the high quality ICs. For example, the test should cover all the likely defects in the design and should avoid the degradation of their design performance, or the design should work within the constraints of the process.

Therefore, this dissertation focuses on the development of new BIST techniques, which a capable of high faults detection including catastrophic and parametric faults. The design strategy is to improve the basic building blocks of BIST, i.e. test stimulus generation, test control, and test response analyzer. All designed BIST is expected to avoid the system performance degradation and to distinguish between good and faulty ICs completely on-chip. The contributions of this dissertation arise from a design of compact and high-speed test stimulus generator, which can reduce the area requirement of BIST circuitry and testing time process. Second, a self-testability system without the stimulus generator is presented in terms of a oscillation-based testing. The proposed system offers a non-instructive source and cover all significant faults in tested ICs. Finally the concept of self-test and calibration is introduced with a capability of preserving an important functional of faulty circuits.

1.5 Dissertation Organization

This dissertation is organized into six chapters. The following chapter 2 presents a full-custom design of chaos-based True Random-Bit Generator (TRBG) implemented on a 0.18-μm CMOS technology with unique composition of three major components, including (i) chaotic jerk oscillator, (ii) $\Delta\Sigma$ modulator, and (iii) simple pre/post-processing. A high-frequency all-CMOS chaotic jerk oscillator has been employed as

a source of randomness. Dynamics properties are described in terms of bifurcation diagram and the Largest Lyapunov Exponents (LLEs) spectrum. The continuous-time 2^{nd}-order $\Delta\Sigma$ modulator has firstly introduced for an increase in a resolution of random bit sequences while an extra clock is not required. Detailed circuit designs for both chaotic jerk oscillator and $\Delta\Sigma$ modulator will be described and the standard statistical measure of randomness will be performed using NIST SP800-22 test suite. The designed chaotic oscillator is utilized as a testing stimulus generator, which can generate testing stimuli automatically and suitable to implement on a single-die chip. Faults detection is achieved through the simple method without requiring any additional digital processing units.

Chapter 3 presents an alternative topology of structural-based testing for the discrete-time $\Delta\Sigma$ modulator. The structure of circuit-under-test is modified and operated as two symmetric structure circuits in the test mode. Different DC offset and simple digital counters are connected to the input and output of the circuit in order to reduce testing process complications and costs, with the modulator operated as a simple signal generator in the test mode. A demonstration of the testing process is performed through the switched-capacitor second-order $\Delta\Sigma$ modulator, which achieves several advantages, including low cost, high-speed testing, and high fault coverage, and covers parametric failure.

Chapter 4 presents the BIST based on a phase difference analysis technique for the analog circuits. The test operation is achieved through the detection of phase shifting between two signals (i.e. the circuit-under-test and the reference clock). The faults signature is simply generated, and diagnosed by digital circuits, including a counter and basic logic components. The test stimulus generation and pass/fail decision are accomplished entirely on-chip, and also offers the range of tolerance in the passive analog components with eliminating the need for the external test equipment.

The BIST method with self-calibration feature for the continuous-time $\delta\sigma$ modulator is introduced in chapter 5. This chapter initially reviews the conventional oscillation testing approaches, and calibration schemes in mixed-signal circuits. The simple circuitry such as a frequency-to-DC circuit, a windows comparator, and basic logic elements are utilized as the faults detection circuits. The calibration system is additionally implemented through the resistor array with a feedback network in order to adjust the gain value of the CUT. Simulation results show the capable of faults detection involves catastrophic and parametric variation. Moreover, the signals-to-noise ratio (SNR) of the CUT can be preserved at the acceptable level against the failure circuitry.

Finally, chapter 6 conclude the overall proposed techniques. The advantages and discussion of all techniques are given. Some potential research directions are recommended as well.

Chapter 2

True Random Bit Generator for High-Speed Testing in $\Delta\Sigma$ Modulator

This chapter presents a full-custom design of chaos-based True Random-Bit Generator (TRBG) implemented on a 0.18-μm CMOS technology with unique composition of three major components, including (i) chaotic jerk oscillator, (ii) $\Delta\Sigma$ modulator, and (iii) simple pre/post-processing. A high-frequency all-CMOS chaotic jerk oscillator has been employed as a source of randomness. Dynamics properties are described in terms of bifurcation diagram and the Largest Lyapunov Exponents (LLEs) spectrum. The continuous-time 2^{nd}-order $\Delta\Sigma$ modulator has firstly introduced for an increase in a resolution of random bit sequences while an extra clock is not required. Detailed circuit designs for both chaotic jerk oscillator and $\Delta\Sigma$ modulator will be described and the standard statistical measure of randomness will be performed using NIST SP800-22 test suite. The compact chaotic oscillator is utilized as a testing stimulus generator, which can generate testing stimuli automatically and suitable to implement on a single-die chip. Faults detection is achieved through the simple method without requiring any additional digital processing units.

2.1 Review on the conventional True Random Bit Generator

Random Bit Generator (RBG) is typically achieved by software-based such as a Linear Congruential Generator (LCG), a Lagged Fibonacci Generator (LFG), and a Linear-Feedback Shift Register (LFSR). As the algorithm-oriented, most of the software-based RBG is defined as a pseudo- random generator, which the randomness is limited by the source generation, resulting in the existence of periodic intervals in the output sequences. Hardware True Random-Bit Generator (TRBG) is a physical process that typically provides a random sequence in which values of bit streams are uniformly distributed over a definite set, and cannot be reliably predicted based on the existing set of values [1]. The hardware TRBG generally represents fundamental cryptographic primitives, and therefore stringent requirements, such as unpredictability and proven statistical standard properties, must be satisfied in order to assure robustness and resistance against attacks [2]. As advanced technologies and expeditious computation have rapidly emerged, the need for robust and high-speed hardware TRBGs has consequently received considerable attention in order to support modern applications such as in security of parallel computing or in real-time data encryptions. [3, 4, 5]

Classical hardware TRBGs are based on stochastic systems that exploit physical phenomenon as sources of randomness such as a jitter noise of clock signals and metastability in circuits [6, 7, 8] or thermal or shot noises obtained from analog devices [9, 10]. However, those classical hardware TRBGs require a properly customized circuitry for randomness extraction. On a contrary to stochastic systems, chaos-based hardware TRBGs are based on a deterministic system in which a source of randomness can be obtained from a well-defined mathematical model, and hence deterministic chaotic circuit. On the one hand, several techniques for chaos-based hardware TRBGs

have recently been proposed through the utilization of Field Programmable Gate Array (FPGA) [11, 12, 13]. Nonetheless, the FPGA is an independently external device that requires an interface to other application processes, and the design process of TRBGs on FPGA is highly complicated due to the proper optimization among various aspects, involving a slice area, RAM, processing speed. Remarkably, the implantation of TRBGs on FPGA is critically depends on a clock frequency, which is a major limitation for gaining high data rate and throughputs.

As an alternative to FPGA, the implementation of chaos-based TRBGs in Application-Specific Integrated Circuit (ASIC) has also received much interest due to a completely embedded security module in physical layer applications. On the one hand, TRBGs based on 3-dimendtional chaotic flow have been reported in two categories, i.e. (i) autonomous flows, including Lorenz [14] and Chen' s systems [15], and (ii) non-autonomous flows, involving a sinusoidal-forced [16] and triangle-wave-based LC chaotic oscillators [17]. These types of TRBGs, however, has a limitation on low output data rate as chaotic flow naturally provides low frequency outputs unless a complex post-processing is exploited. On the other hand, TRBGs based on 1-dimendtional chaotic maps have extensively been proposed such as those of utilizing Bernoulli shift map [18], Sawtooth map [19], or Approximate V-shape map [20]. Despite the fact that chaotic maps are simple in terms of circuit implementation and capable of generating higher frequency than that of chaotic flows, either switched-capacitor [21] or switched-current [22] are essentially required and hence a clock frequency becomes a critical issue as FPGA.

Recently, attempts for implementing high-speed and high-data-rate chaos-based TRBGs based on Analog-to-Digital Converters (ADC) as an interface between a source of randomness and a post-processing unit have been suggested. The modified multi-stage pipeline ADCs as a chaotic source using 0.18-μm CMOS based TRBGs [23] provides

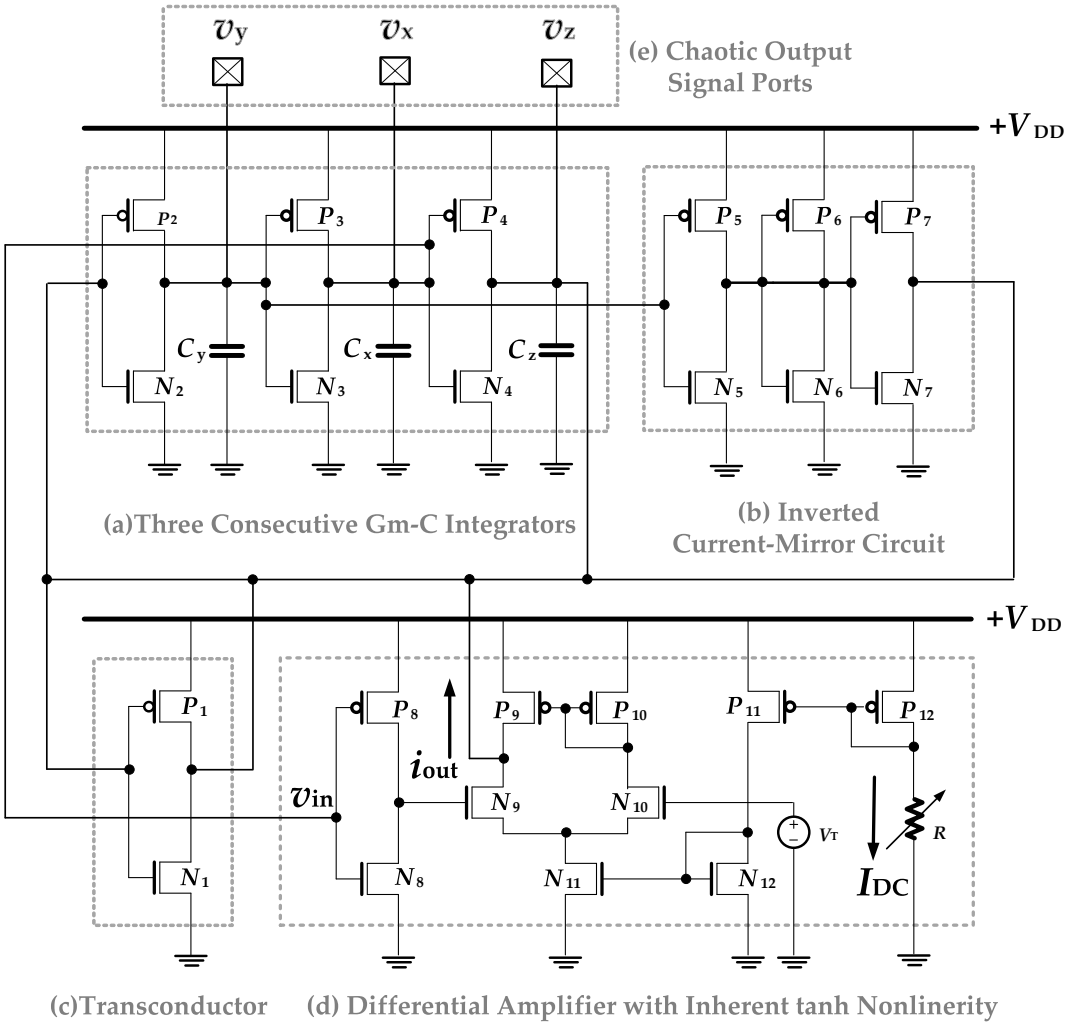

Fig. 2.1 The proposed circuit configuration of chaotic jerk oscillator.

an output rate of 40 Mbit/s and another TRBGs constructed by a Photonic Integrated Circuit (PIC) that emits broadband chaotic signals provides extremely high data rate of 140 Gb/s [24]. Despite a high data rate, the multi-stage pipeline ADCs is complicated requiring a number of components whilst the PIC is expensive and suitable for specific applications such as in communication systems.

2.2 An Autonomous Chaotic Jerk Model

An autonomous chaotic system has been an active subject in the fields of physics since the first discovery by Lorenz in 1963 [25]. The system has illustrated by a set of third-order ordinary differential equations (ODE), showing in the three-dimensional phase-space domain and requires at least one non-linearity function. In addition, an explicit form of third-order ODE has been reported in 1996 [26], called "jerk function". It can be written as $\dddot{x} = J(x, \dot{x}, \ddot{x})$, which represents the derivative of acceleration. The jerk form of chaotic systems has gained great attention due to its showing in the form of the single dynamical system. The particular advatage of a jerk form is a capability of investigating chaotic dynamics through damping coefficients in a single equation.

Although the chaotic dynamics can be analyzed regarding numerical and demonstrated by a computational tool, the appropriate condition for ensuring the chaotic phenomenon in real nature is to implement in electronic devices. Several approaches have been investigated the simple term of chaotic jerk equations [27, 28, 29] in order to minimize the circuit components. However, even simple jerk equation may lead to a complex circuit due to the non-linearity function, e.g., an exponential , absolute and power function [30, 31, 32].

The simple model of chaotic jerk system with double-score-like behavior is presented in this Section. Implementation of CMOS architecture with adjustable attractor feature is also described through the numerical analysis and simulation in the circuit level.

2.2.1 All-CMOS Chaotic Jerk Oscillator

A typical chaotic jerk oscillator is a three-dimensional chaotic system, and can generally be described by a mathematical model in the case where a nonlinear function

is in an x term with first-order polynomial included as follows

$$\dddot{x} = a_6\ddot{x} + a_5\dot{x} + a_4x + a_3f\left(a_2x + a_1\right) + a_0 \tag{2.1}$$

where a_i, $i = 0, 1, 2...6$, is a coefficient. Based upon Eq. (2.1), Fig. 2.1 subsequently depicts a realization of a simple all-CMOS chaotic jerk oscillator through inherently hyperbolic tangent nonlinearity in an operational amplifier (Opamp). It can be considered in Fig. 2.1, two essential building blocks are (i) the three consecutive integrators for composition of a third-order chaotic flow, and (ii) a differential amplifier that inherently provides Hyperbolic Tangent (tanh) nonlinearity. Additionally, a transducer and a current-mirror circuit are necessarily required in order to fulfill chaos dynamics. As for circuit simplicity purposes, on the one hand, most building blocks were implemented based on a simple inverter comprising a typical complementary nMOS and pMOS. The inverter operating in a saturation mode typically provides a transconductance gain G_m as follows

$$G_m = \mu_nC_{OX}\frac{W_n}{L_n}\left(V_{GS} - V_{THn}\right) + \mu_pC_{OX}\frac{W_p}{L_n}\left(V_{GS} - V_{THp}\right) \tag{2.2}$$

where μ_n and μ_p are electron mobility of nMOS and pMOS transistors respectively. C_{OX} is an oxide capacitance. W and L are width and length of a transistor. The voltage V_{GS} is a gate-source voltage of a transistor. The voltages V_{THn} and V_{THp} are threshold voltages of nMOS and pMOS transistors, respectively. On the other hand, the differential amplifier employs two nMOS transistors N_9 and N_{10} as a differential input pair, and exploits two pMOS transistors P_9 and P_{10} as an active load in a current-mirror configuration in order to provide a single-ended output. Assuming a differential input pair is operated in a saturation region, the voltage-to-current transfer characteristics, i.e., $i_{out} = f\left(v_{in}\right)$, can approximately be described in piecewise-linear nonlinear model using the square law as follows

$$i_{out} = \begin{cases} \frac{1}{2}\mu_nC_{OX}\frac{W_9}{L_9}V_i\sqrt{2K^2 - v_{in}} & ,|v_{in}| \leq K \\ I_{DC}sgn\left(v_{in}\right) & ,|v_{in}| > K \end{cases} \tag{2.3}$$

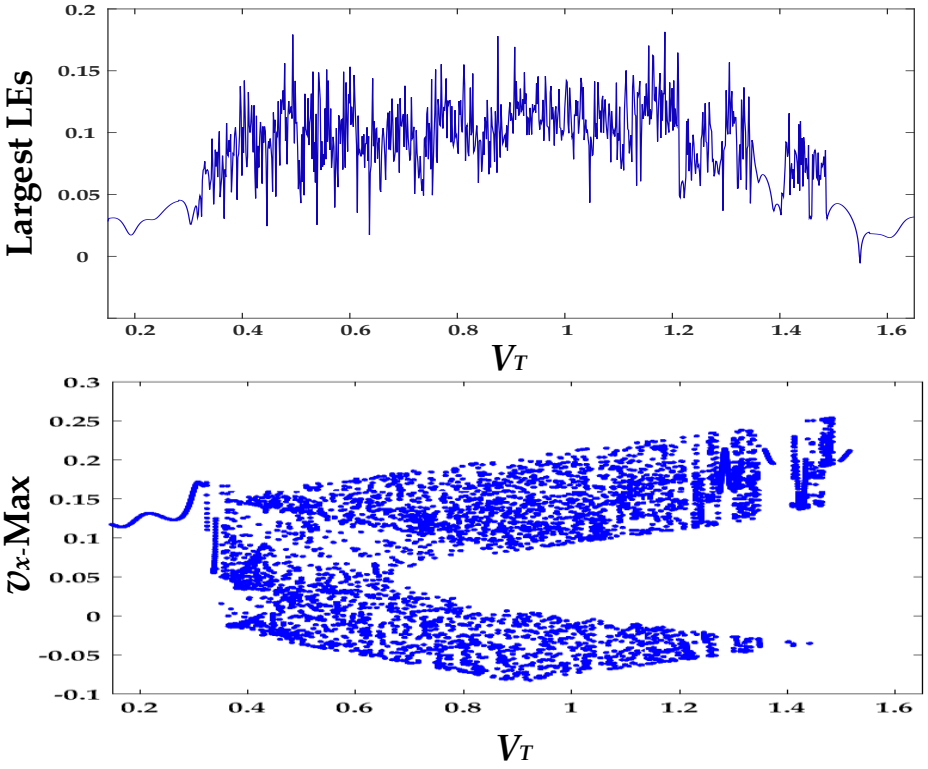

Fig. 2.2 Plots of the spectrum of LLEs and Bifurcation diagram of X_{max} over a tuning voltage V_T.

where sgn(v_{in}) is a Signum function and K is a constant defined as

$$K = \sqrt{\frac{2I_{DC}}{\mu_n C_{OX} \frac{W_9}{L_9}}} \tag{2.4}$$

For purpose of simplicity, the values of W and L of both pMOS and nMOS transistors were set to be equal, and hence the transconductance G_m is therefore equal for all inverters. A mathematical model of the proposed CMOS chaotic jerk oscillator in Fig. 2.1 can be formulated through a classical circuit analysis using Kirchhoff' s law, and the results reveal the system of Ordinary Differential Equations (ODEs) as follows

$$\begin{aligned} \frac{dv_x}{dt} &= -\frac{G_m}{C_x} v_y \\ \frac{dv_y}{dt} &= -\frac{G_m}{C_y} v_z \\ \frac{dv_z}{dt} &= -\frac{G_m}{C_z} v_x + \frac{G_m}{C_z} v_y - \frac{G_m}{C_z} v_z + \frac{f\,(v_x)}{C_z} \end{aligned} \tag{2.5}$$

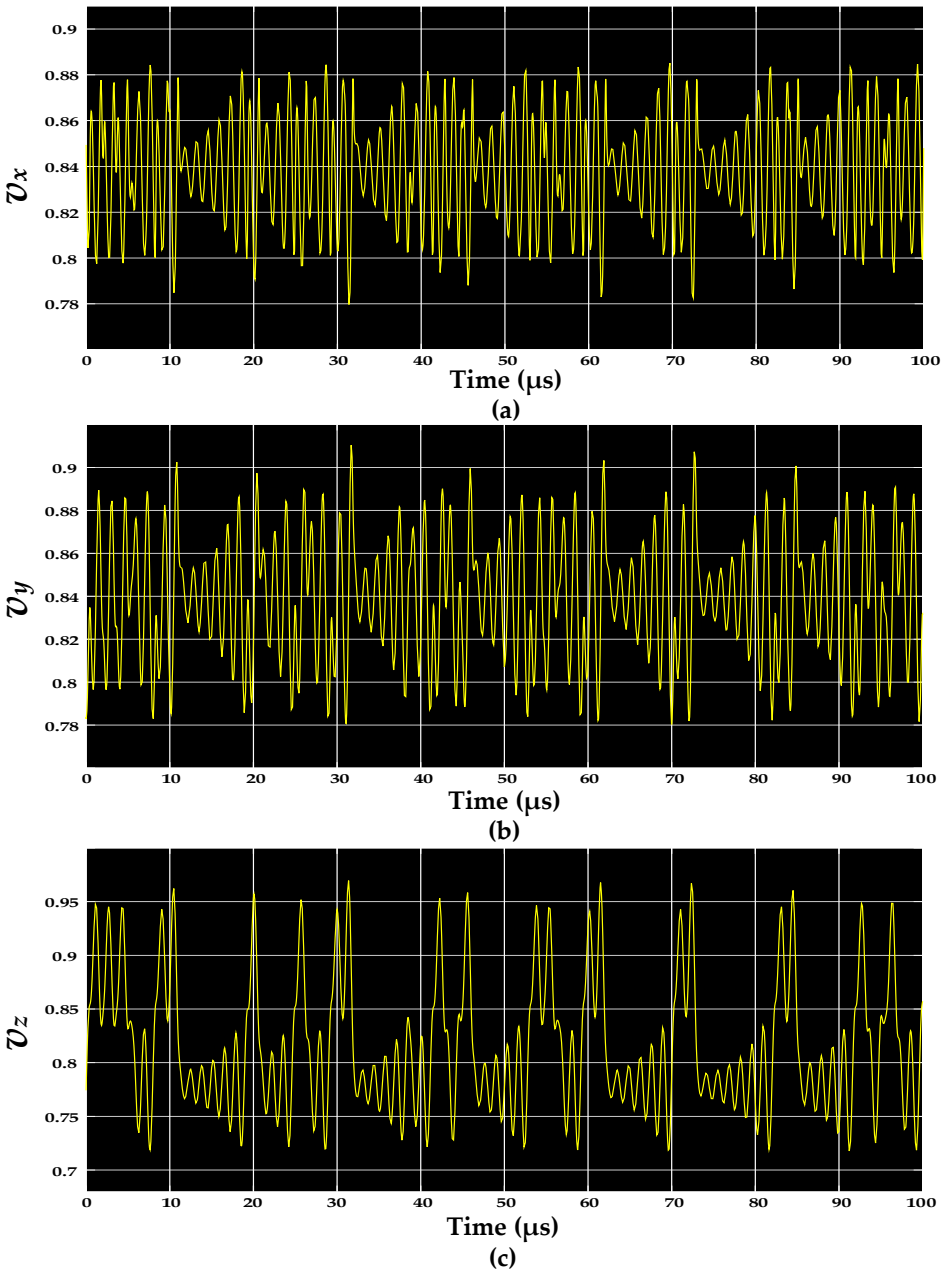

Fig. 2.3 Chaotic waveform in time-domain of (a) v_x, (b) v_y, and (c) v_z at $V_T = 0.9V$.

where the nonlinear function $f(v_x)$ is a hyperbolic tangent function expressed as

$$f(v_x) = I_{DC} tanh(b_1(b_2 v_x - V_T)) \tag{2.6}$$

where a constant b_1 is a scaling factor of a typical *tanh* function while a constant b_2 a voltage gain. In this particular design, the capacitor C_z is unique while the capacitors

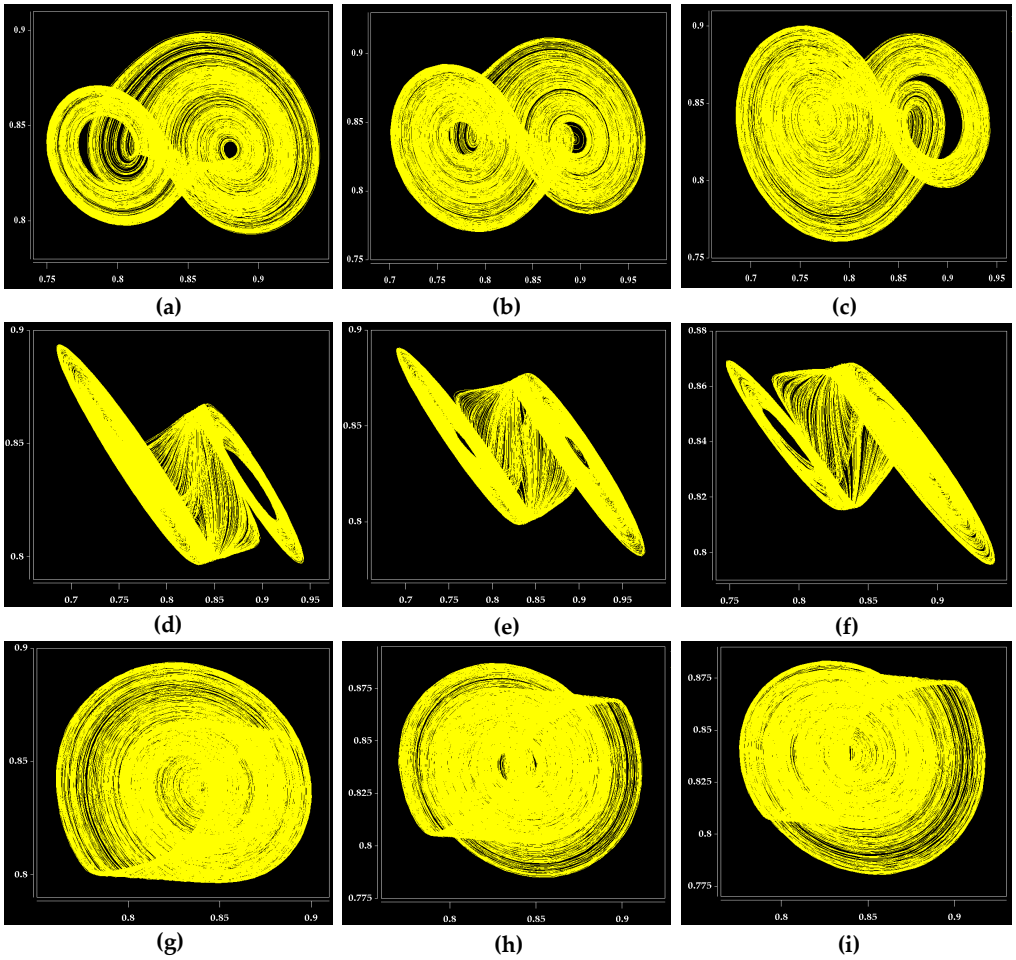

Fig. 2.4 Two-dimensional strange attractor with different tuning the voltage V_T obtained from the proposed oscillator, between (a-c) v_x - v_y, (d-f) v_x - v_z, (g-i) v_y - v_z.

C_x and C_y are equal, and therefore C_{xy} is denoted in a manner that $C_{xy} = C_x = C_y$. The time constant $\tau = C_{xy}/G_m$. The system characteristics can be changed by the DC tuning voltage V_T. A dimensionless system of Eq. (2.5) is summarized in a matrix form described in Eq. (2.7), comprising normalized variables (X, Y, Z), system constants (A, B, C), and an arbitrary reference voltage V_r.

$$\begin{bmatrix} \dot{X} & X & A \\ \dot{Y} & Y & B \\ \dot{Z} & Z & C \end{bmatrix} = \begin{bmatrix} \frac{dX}{d\tau} & \frac{v_x}{V_r} & \frac{C_{xy}}{C_z} \\ \frac{dY}{d\tau} & \frac{v_y}{V_r} & \frac{C_{xy} I_{DC}}{G_m V_r C_z} \\ \frac{dZ}{d\tau} & \frac{v_z}{V_r} & \frac{V_T}{V_r} \end{bmatrix} \tag{2.7}$$

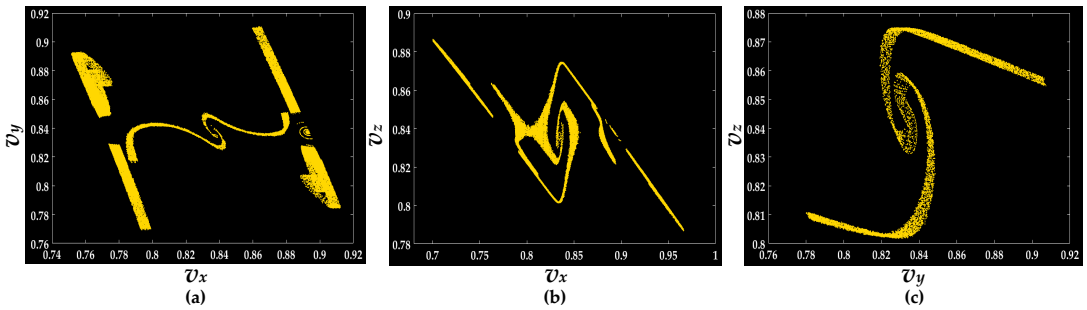

Fig. 2.5 Poincarè mapping in planes where (a) $v_z = 0.84$, (b) $v_y = 0.84$, and (c) $v_x = 0.84$.

$$\begin{bmatrix} \dot{X} \\ \dot{Y} \\ \dot{Z} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 0 & 0 & -1 \\ -A & A & -A \end{bmatrix} \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ Btanh\left(b_1\left(b_2X - C\right)\right) \end{bmatrix} \tag{2.8}$$

Transformation of a dynamical form in Eq. (2.8) into a jerk equation results in a following form

$$\dddot{X} = -A\left(\ddot{X} + \dot{X} + X\right) + Btanh\left(b_1b_2X - b_1C\right) \tag{2.9}$$

Eq. (2.9) also apparently satisfies mathematical model as previously described in a generic jerk form in Eq. (2.1) with following coefficients, i.e., a_6 = -A, a_5 = -A, a_4 = -A, a_3 = B, $a_2 = b_1b_2$, $a_1 = b_1C$, and $a_0 = 0$.

2.2.2 Chaotic Dynamics Evaluation

In order to investigate chaotic dynamics from the proposed oscillator, solutions of the jerk Eq. (2.9) were simulated in MATLAB using the 4^{th}-order Runge-Kutta integration algorithm with a step size of 10^{-3} and the initial condition was set at (0.01, 0, 0). The parameters W_n and L_n of all nMOS transistors are 1μm and 0.36μm, respectively. Meanwhile, the parameters W_p and L_p of all pMOS transistors are 2.4μm and 0.36μm, respectively. The resulting transconductance of inverters G_m is equal to 288μS. The capacitors were specifically customized to C_{xy} = 10pF and C_z = 20pF. The DC current was set to I_{DC} = 26μA. The constant parameters b_1 and b_2 were appropriately fixed to 500 and 15, respectively. A bifurcation diagram of X_{max} and

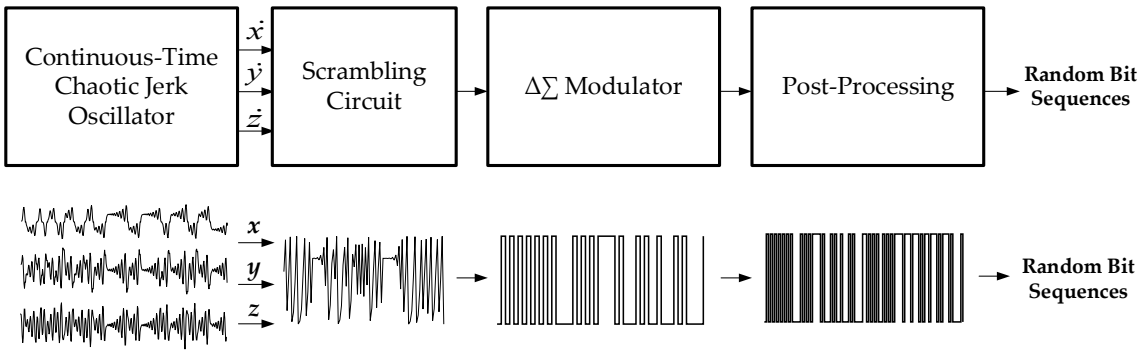

Fig. 2.6 Block diagram of the proposed TRBG with $\Delta\Sigma$ modulation of chaotic jerk signals.

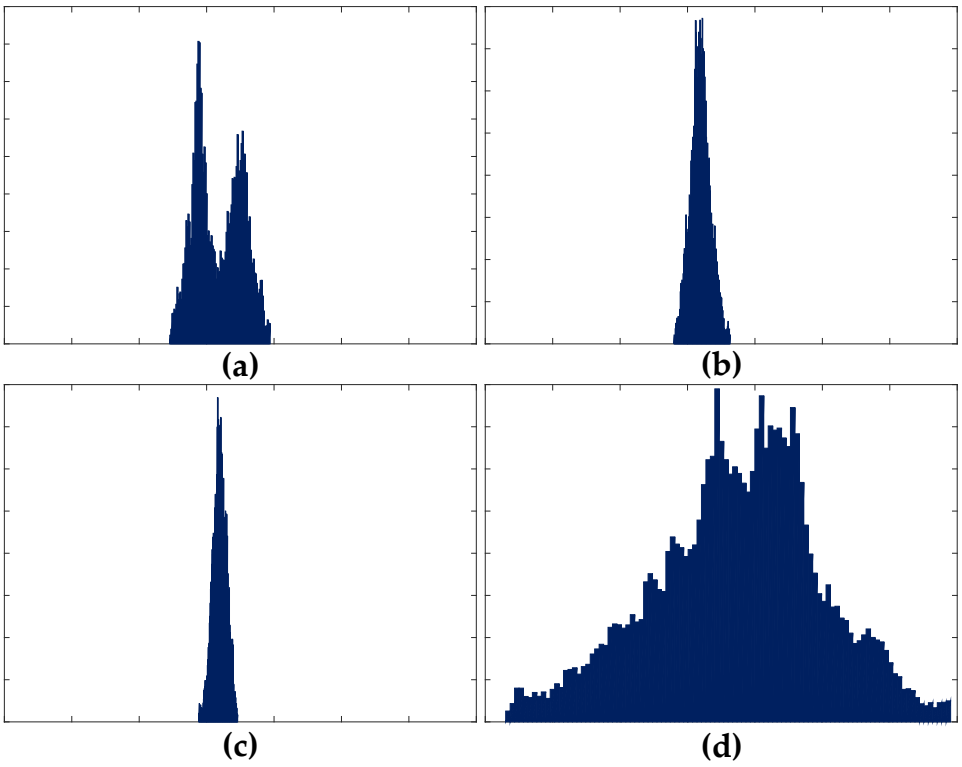

Fig. 2.7 Histograms of the chaotic jerk signals at (a) v_x, (b) v_x, (c) v_x, and (d) after scrambling process.

LLEs spectrum were simulated, as a qualitative and quantitative measurements, by tuning the voltage V_T from 0.15V to 1.65V in 1,000 steps. The LLEs is a quantity that characterizes the rate of separation of infinitesimally close trajectories, expressed as

$$LE = \lim_{n\to\infty} \frac{1}{N} \sum_{n=1}^{N} log_2 \frac{dX_{n+1}}{dX_n} \tag{2.10}$$

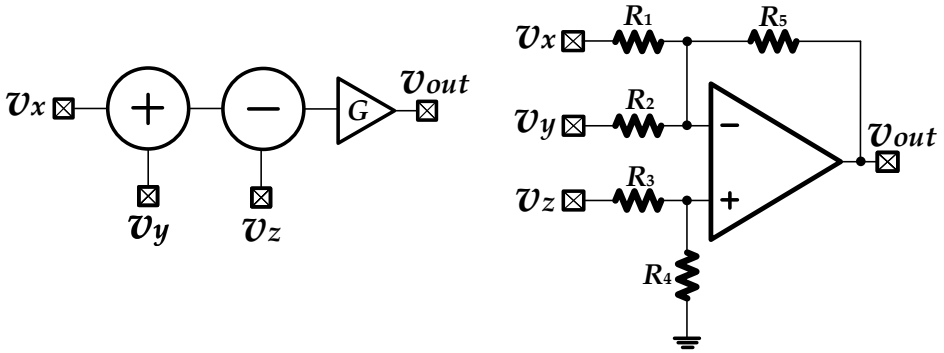

Fig. 2.8 Block diagram and a circuit of the signals scrambling technique.

where N is the number of iterations. Fig. 2.2 illustrates the bifurcation diagram of X_{max} against voltage V_T, where the variety of dynamics are obviously exhibited on the dense region (0.3 - 1.38). In addition, the chaotic dynamics in such region are also indicated by the positive values of the LLEs spectrum. Fig. 2.3 shows signals waveform in time-domain of v_x, v_y and v_z at $V_T = 0.9$V, which apparently exhibit a nonlinear behavior.

In addition, the proposed CMOS chaotic jerk oscillator has been implemented using Cadence virtuoso environment with 0.18-μm Rohm CMOS technology. Fig. 2.4 shows the balanced-to-unbalanced transition of double-scroll attractors on node v_x - v_y (a-c), v_x - v_z (d-f), and v_y - v_z (g-i), where the tuning voltage V_T is varied from 0.7V to 1.05V. Fig. 2.5(a), (b), and (c) show the Poincarè mapping in 2-dimensional plane where $v_z = 0.84$, $v_y = 0.84$ and $v_x = 0.84$, respectively. The tuning voltage V_T is set to 0.9. It is noticeable form the trajectories that this system exhibits the symmetrically double-scroll dynamics with the equilibrium point at 0.84V. It is clearly seen that the proposed oscillator is a capable of an autonomous generating smooth transitions from a balanced double-scroll jerk attractor to an unbalanced double-scroll, and additionally to either a right-half or a left-half single-scroll attractor by varying a DC tuning voltage. The proposed CMOS chaotic jerk oscillator operates at 1.8-V single supply voltage and

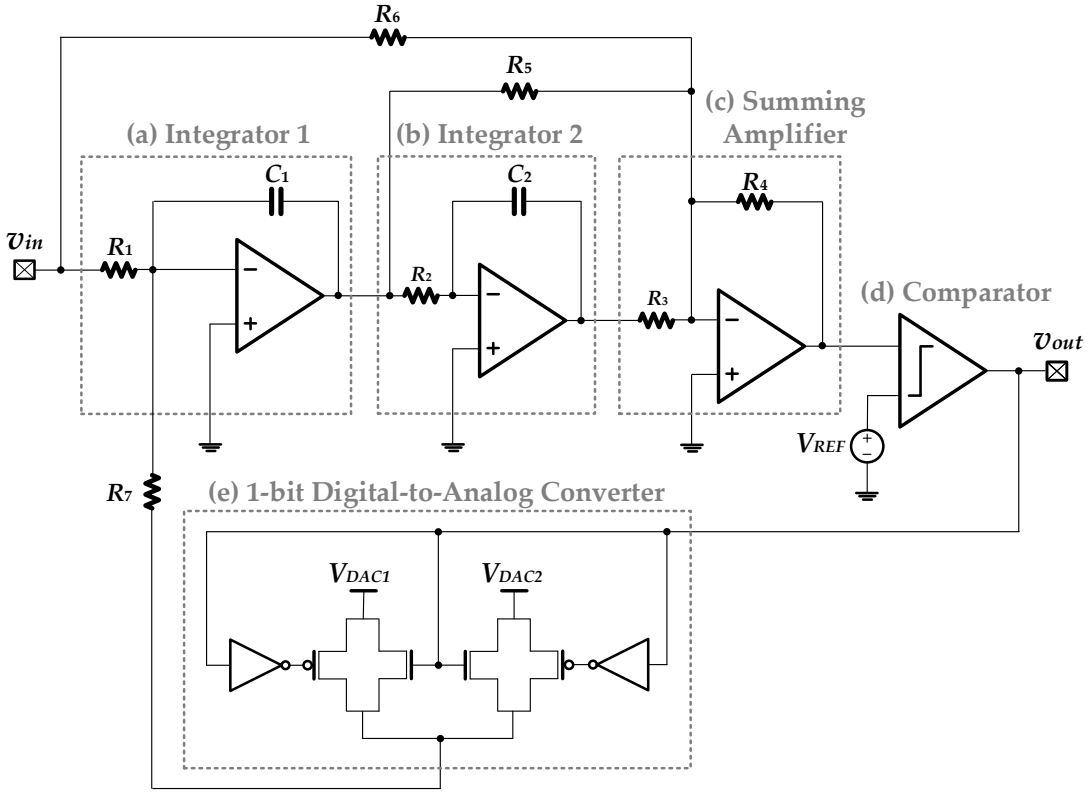

Fig. 2.9 The single-bit second-order ΔΣ modulator with feed-forward topology.

the power dissipation is 0.72 mW.

2.3 Proposed Architecture of a TRBG through ΔΣ Modulation of Chaotic Jerk Signals

The overall system of the proposed TRBG with ΔΣ modulation of chaotic signals is illustrated in Fig. 2.6. The system comprises four important components, i.e. the continuous-time chaotic jerk oscillator, a simple scrambling signals circuit, a ΔΣ modulator, and a post-processing circuit. The non-deterministic chaotic signals are generated automatically by the chaotic jerk oscillator as the source of the TRBG. Utilization of the chaos-based oscillator has gained numerous advantages such as elimination a complex structure of the signal generators, a nondeterministic entropy source, and the truly

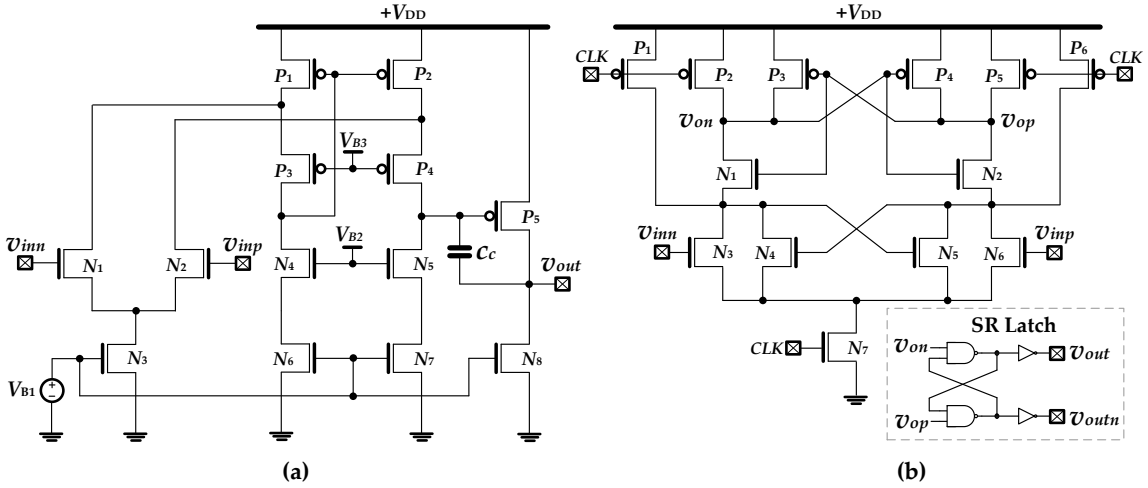

Fig. 2.10 (a) Folded-cascode operational transconductance amplifier and (b) a dynamic comparator.

randomness property based on physical phenomenon. However, a crucial issue is the synchronization property of chaotic dynamics, i.e. the behavior of two or more chaotic systems, either equivalent or nonequivalent, might be synchronized by linking them with common signals [33].

The output sequences might be predicted by a mimic system using master-slave synchronization scheme [34]. Thus, a pre/post-processing method is necessary for TRBG in order to fulfill the imperfections of the chaotic property. The chaotic signals of each output nodes (v_x, v_y, v_z) are merged together by the scrambling circuit as a simple pre-processing technique. Lastly, the randomness of binary sequences is enchanted by the digital post-processing stage based on the structure in [35].

In order to increase the data rate, the continuous-time ΔΣ modulator is employed with high sampling frequency. Oversampling property is the major key to achieve the higher transmission rate. Otherwise, using an embedded quantizer in a feedback loop and applying a signal processing technique, therefore increasing the output resolution. This section presents an architecture of the proposed TRBG in terms of the circuit realization. The overall circuits are implemented on 0.18-μm CMOS standard technology.

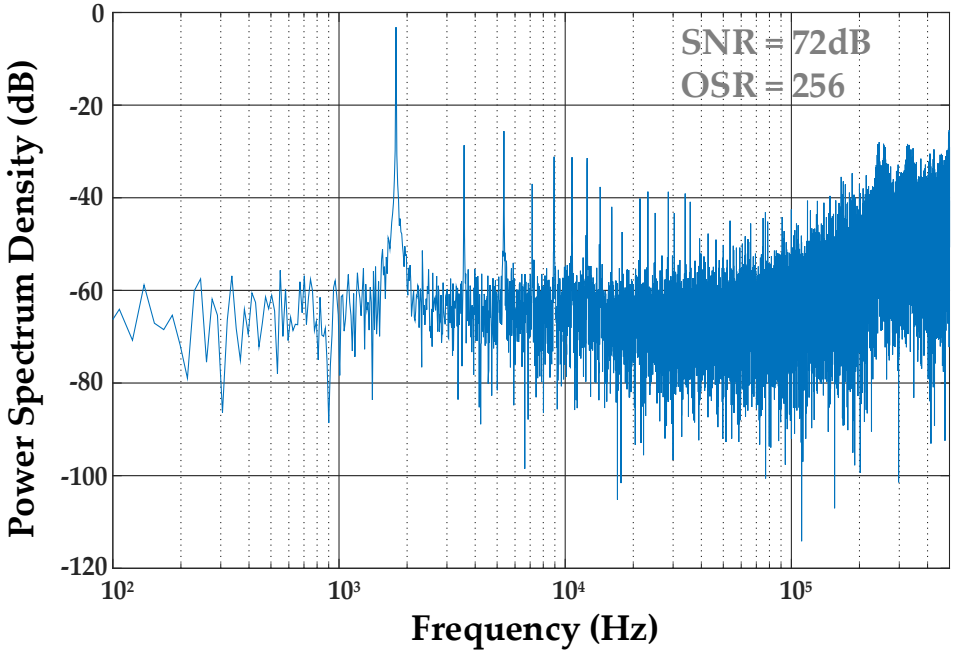

Fig. 2.11 Output power spectrum density of the modulator.

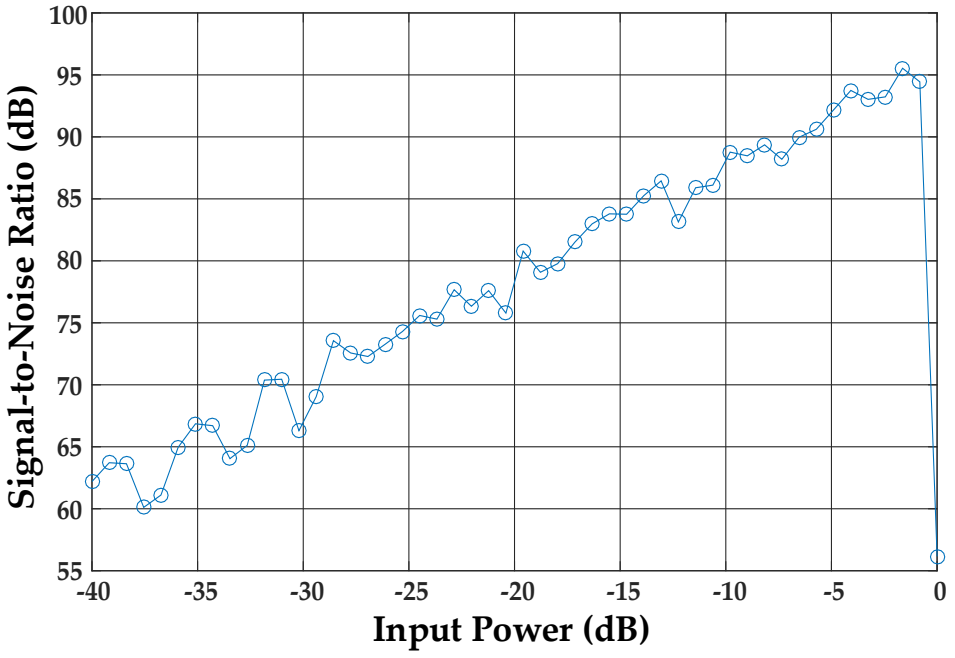

Fig. 2.12 Signal-to-noise ratio as a function of normalized input power.

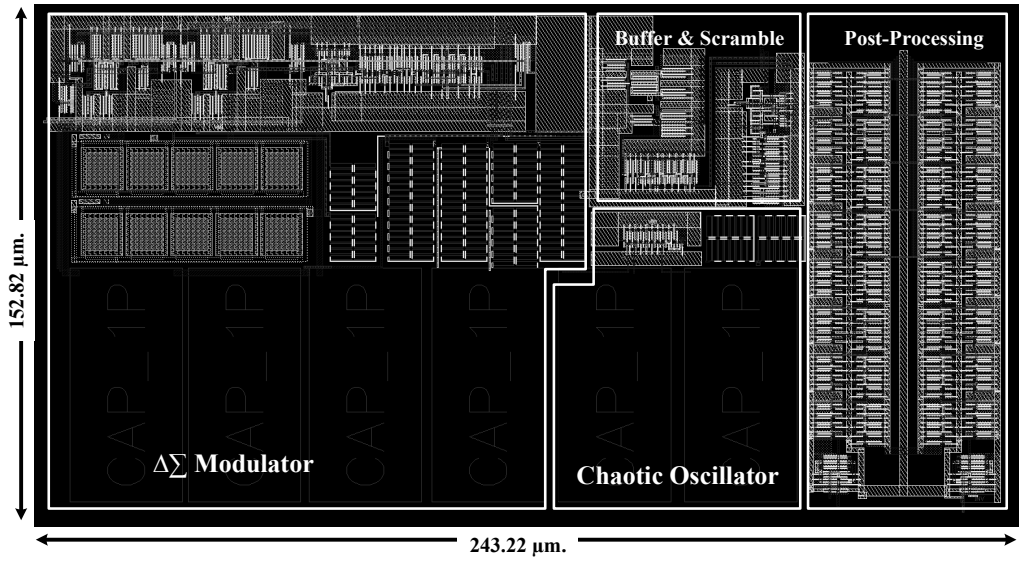

Fig. 2.13 Layout diagram of overall circuits in 0.18-μm CMOS standard technology.

2.3.1 Signals Scrambling Circuit

A scrambling signals technique is typically utilized in a secure communication system in order to avoid the periodic data and to smoothly combine the frequency smoothly over the available bandwidth. Fig. 2.7(a), Fig. 2.7(b), and Fig. 2.7(c) show the output histogram of the chaotic jerk oscillator at nodes v_x, v_y, and v_z, respectively. It is clearly seen that the amplitude of each node is indicated in the narrow range of bandwidth (less than $0.4V_{pp}$), which is undesirable for the TRBG. Therefore, the scrambling technique is used, as the pre-processing method, to intergrade the three output nodes (v_x, v_y, and v_z) into a single output node, and expand the amplitude range of the chaotic jerk oscillator. The method is achieved by the three operations, i.e. summing, subtraction, and amplifying, and can be implemented by a simple circuit. Fig. 2.8 depicts a block diagram and a circuit of the proposed scrambling technique, where $R_1 = R_2 = R_3 = R_A$ and $R_4 = R_5 = R_B$, the output of the circuit can be expressed as

$$v_{out} = \frac{R_B}{R_A}\left[(v_x + v_y) - v_z\right] \tag{2.11}$$

Fig. 2.7(d) illustrates the output histogram after scrambled signals, when R_A and R_B are fixed as 20kΩ and 50kΩ, respectively. The histogram indicates higher distribution of the output amplitude, which is a require property of the TRBG.

2.3.2 The Continuous-Time ΔΣ modulator

Unlike a discrete-time system, which the switched-capacitors is a major component for sampling operation, the continuous-time design places the input sampling just before the quantizer. Consequently, a non-overlapping clock generator is not required and the system throughput can be determined by maximum sampling rate of the quantizer (comparator). Without the switched-capacitors, the continuous-time consume less power than the discrete-time system and also easy to drive form external input with high bandwidth. Fig. 2.9 shows the second-order continuous-time ΔΣ modulator with feed-forward topology. The circuit comprises two RC integrators, a summing amplifier, a comparator as 1-bit quantizer, and 1-bit digital-to-analog converter (DAC). The feed-forward topology is used in order to decrease a harmonic distortion and increase a signal-to-noise ratio (SNR). The output of the modulator in z-transform is given by

$$v_{out}(z) = \frac{v_{in}\left[z^{-2}\left(a_1a_2c_1 - a_1c_2\right) + a_1c_2z^{-1}\right] + Q\left(1 - z^{-1}\right)}{z^{-2}\left(a_1a_2c_1 - a_1c_2 + 1\right) + z^{-1}\left(a_1c_2 - 2\right) + 1} \tag{2.12}$$

where Q(z) is the quantization error of the modulator. The parameter a_1, a_2, and c_1, c_2 represent integrator gain and the feed-forward gain, respectively. The operational transconductance amplifier (OTA) is the core component whose implementation determines the performance of the ΔΣ modulator. Basically, the dominant specifications that affect the modulator performance comprise the bandwidth, speed, and stability, where a 60dB DC gain is adequate. A two-stage OTA is commonly used with Miller compensation. This can provide a high speed and high output swing but suffers from a poor power-supply rejection ratio (PSRR) and high power consumption. Another

drawback is a difficulty in detecting parametric faults, which is due to the internal compensation components (e.g., resistor and capacitor). These limited performances can be compensated for by a folded-cascode OTA, which offers good input common-range, self-compensation, and high DC gain. A high-performance, folded-cascode OTA is utilized as illustrated in Fig. 2.10(a). The differential-output DC gain and the power dissipation can be given by

$$A_{DC} = \alpha\,(1+\lambda)\,(G_{mn} r_{DSn}) \tag{2.13}$$

$$P_{diss} = (I_3 + I_6 + I_7 + I_8)\,(V_{DD} + |V_{SS}|) \tag{2.14}$$

where α and λ are the relative values of N- and P-transistor transconductance and the current flows in M_8, respectively. The simulation results from HSPICE software implies that the designed OTA can achieve a unity gain bandwidth (GBW) more than 60MHz with load capacitance of 1pF and phase margin of 83°. The DC gain of the Opamp is higher than 64dB at 30μA bias current and the measured power dissipation is approximately 0.19mW.

The comparator is the secondary major component that affects the modulator performance. The requirements of this block are flexible, since the performance of the modulator is nearly insensitive to the comparator offset and hysteresis function. The dynamic comparator with SR latch is considered as a single-bit quantizer, as shown in the Fig. 2.10(b). In order to achieve low power and high sampling rate, the circuit structure is designed based on Rahman et al. [36]. In this topology, symmetric structural with regenerative feedback is the major issue. This comparator dissipates at approximately 0.15mW with 50MHz of maximum sampling rate. The transistor aspect ratio of the overall sub-circuits is also shown in Table 2.1.

The performance of the proposed ΔΣ modulator was validated through a HSPICE environment operated in the ordinary condition. The sinusoidal input at 1.785kHz was used with a 1MHz sampling frequency. Fig. 2.11 exhibits the simulated power spectrum

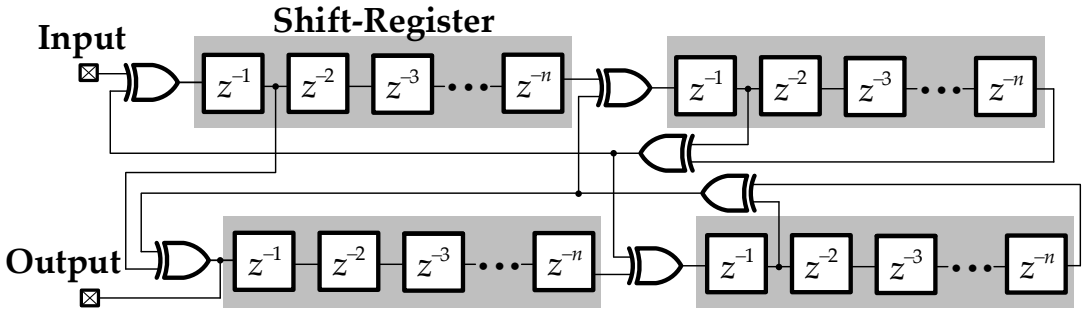

Fig. 2.14 Post-processing unit structure.

density (PSD) where a 65,536-points FFT with simple rectangular truncation window. The behavior of the SNR with of the input power is also shown in Fig. 2.12 where the maximum SNR was 96dB and almost reached 14 bits of the effective number of bits (ENOB). Meanwhile, the overall power consumption as measured was less than 0.6mW and dominated by the operational amplifier (0.19mW). It can be seen that the proposed ΔΣ modulator achieves the power efficiency and acceptable performances widely found in commercial applications. Fig. 2.13 shows the layout diagram of overall circuits in 0.18-μm CMOS standard technology.

2.3.3 Post-Processing Unit

Although, the chaotic-based entropy source provides a highly dynamic and unpredictable behavior, which are the applicable property of TRBG. However, the pure output of entropy source tends to be deviated from the true-randomness property over long-time. Therefore, the post-processing unit is typically required to reduce or remove such deviations, while still maintaining its generation bit-rate. Fig. 2.14 depicts the post-processing unit structure based on a Von Neumann Corrector [35]. The unit structure comprises four shift-registers which is connected by the Exclusive OR (XOR) logic operations. The delay stages (n) of the shift-registers is fixed to 8 and can be simply implemented by a Flip-Flop or latch. The XOR operation of the shift-register with

Table 2.1 Transistor aspect ratio of the designed ΔΣ modulator.

MOS Transistors		**Aspect Ratio (W/L)**
Op Amp	P_1-P_2	180
	P_3-P_4	90
	P_5	296
	N_1-N_2	40
	N_3	20
	N_4-N_7	80
	N_8	150
Comparator	P_1-P_2	12
	P_3-P_4	4
	P_5-P_6	12
	N_1-N_2	4
	N_3-N_6	8
	N_7	12

slightly different delay prevents an overlapping bits-pair (e.g., “0000” or “1111”) and performs an equal amount of bit “0” and “1”.

2.4 True Random Bits Generator Evaluation

Since the proposed TRNG is based on the chaotic source, the output bit sequences significantly imply the chaotic properties, which is a sensitivity to the initial condition, unpredictable, and deterministic. However, those properties do not indicate the randomness of the output bit sequences. The quality of TRBG typically depends on the statistical properties of the generated bit sequences, e.g. randomness, unpredictability, and correlation. In this section, entropy and two correlation testing methods have been used for a qualitative analysis. In addition, the most well-known quantitative method, i.e., the National Institute of Standards and Technology (NIST) Statistical Test Suite,

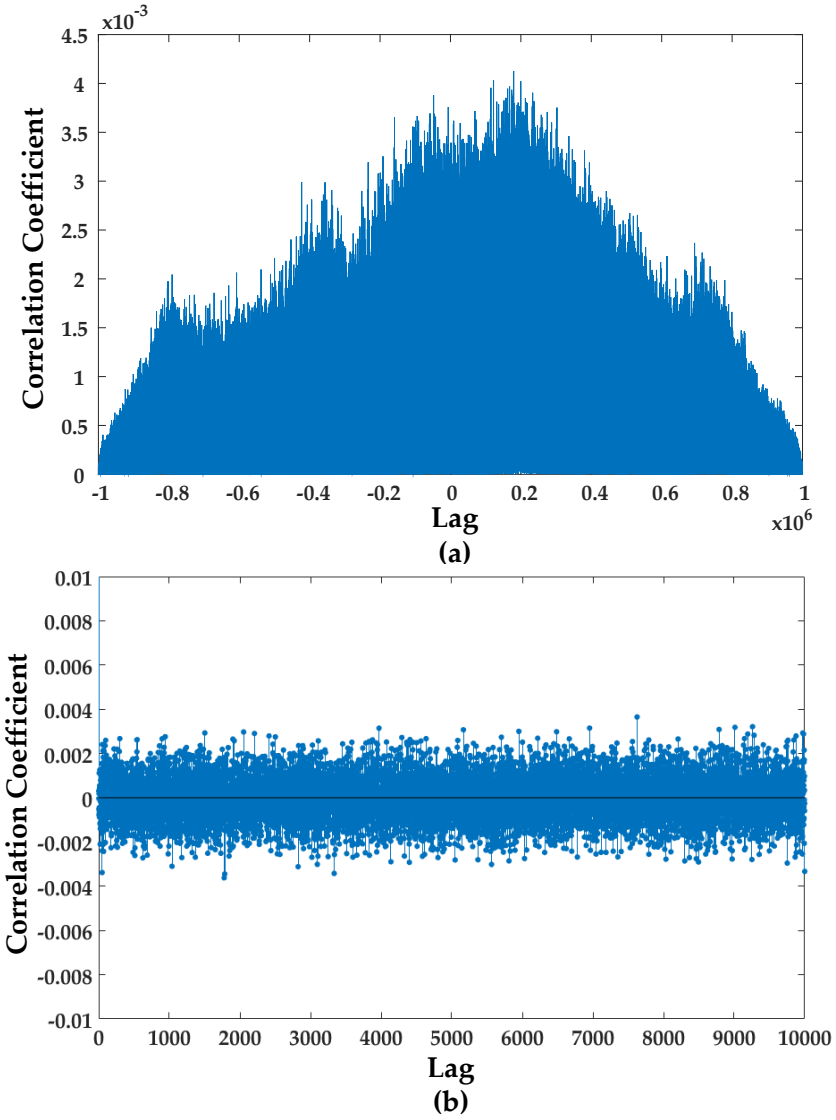

Fig. 2.15 Correlation analysis between the output binary sequences, (a) normalized cross-correlation, and (b) autocorrelation.

has been employed.

2.4.1 Cross-Correlation, Autocorrelation and Entropy

The cross-correlation function is a standard method for measuring the similarity between two time-series sequence. The input binary sequences are compared to identify a bit pattern that repeating in the time-series, known as a matching template algorithm.

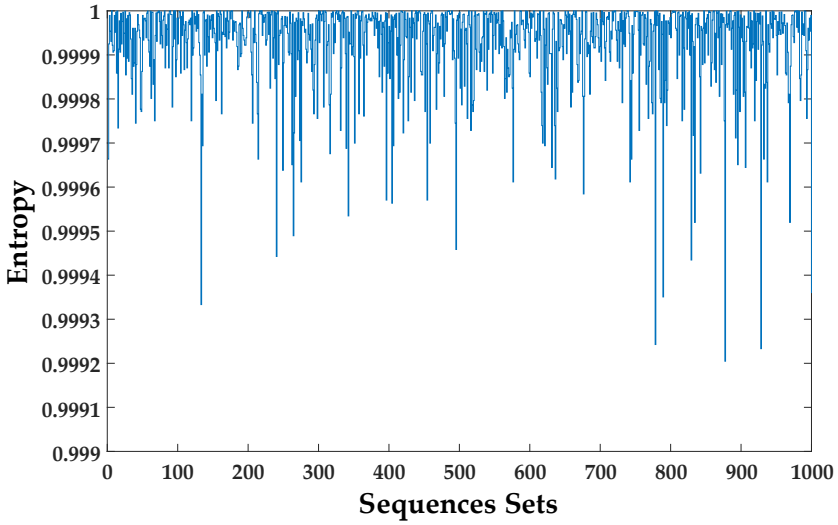

Fig. 2.16 The entropy of difference 1,000 sets of the output binary sequences.

The cross-correlation can be described as follows

$$r_{xy}(\tau) = \int_{-\infty}^{\infty} x(t)\, y(t+\tau)\, dt \tag{2.15}$$

where $r_{xy}(\tau)$ represents a correlation coefficient of the time lags. The function $x(t)$ and $y(t)$ are the different time-series sequences. This function can also be normalized as

$$\overline{r}_{xy}(\tau) = \frac{|r_{xy}(\tau)|}{\sqrt{|r_{xx}(0)|\,|r_{yy}(0)|}} \tag{2.16}$$

where $\overline{r}_{xy}(\tau)$ is a normalized quantity in range -1 and 1. Likewise, an autocorrelation is the correlation with delayed between the value in the same time-series as follows

$$r_{xx}(\tau) = \int_{-\infty}^{\infty} x(t)\, x(t+\tau)\, dt \tag{2.17}$$

Typically, the unity value of correlation coefficient ($r = 1$) indicates the exactly similar at alignment of two time-series, whereas the $r = 0$ suggests that those sequences are uncorrelated together. Fig. 2.15(a) exhibits the normalized cross-correlation of two 1,000,000 binary sequences, where the autocorrelation of 1,000,000 binary sequences form the proposed system is shown in Fig. 2.15(b). It is apparent from the normalized cross-correlation and autocorrelation that the output binary sequences are practically

Table 2.2 Summary of NIST standard test results of 1,000,000 binary sequences of 30 proportions.

Test Methods	**Proportion**	**P-values**	**Results**
Frequency Test	1.00	0.6128	Success
Block Frequency	1.00	0.8254	Success
Runs	1.00	0.2668	Success
Longest Run of Ones Block	1.00	0.9364	Success
Binary Matrix Rank	0.97	0.8626	Success
Discrete Fourier Transform	0.97	0.4517	Success
Non-overlapping Template Matching (148 tests)	1.00	0.4969*	Success
Overlapping Template Matching	0.97	0.7078	Success
Universal Statistical	1.00	0.3854	Success
Linear Complexity	1.00	0.6105	Success
Serial 1	1.00	0.9828	Success
Serial 2	0.97	0.2787	Success
Approximate Entropy	1.00	0.8535	Success
Cumulative Sums (2 tests)	1.00	0.7264*	Success
Random Excursions (8 states)	1.00	0.3077*	Success
Random Excursions Variant (18 states)	1.00	0.3330*	Success

* = Average P-values.

uncorrelated and rarely occurred the periodic region due to the correlation coefficients of two functions are relatively close to zero for entire values. Moreover, the entropy of thousand sets of 10,000 binary sequences have been investigated based on Shannon' s entropy as illustrated in Fig. 2.16. As expected, the entropy values have reached the

Table 2.3 Summary of Alphabit battery.

Test Methods	**Parameter**	**Proportions**
smultin_MultinomialBitsOver	L=2	30/30
	L=4	30/30
	L=8	30/30
	L=16	30/30
sstring_HammingIndep	L=16	30/30
	L=32	29/30
sstring_HammingCorr	L=32	30/30
swalk_RandomWalk1	L=64	30/30
	L=320	30/30

unity for all sets of the output binary sequences which implies the high randomness property of entire sequences.

2.4.2 NIST SP800-22 Standard Test Suite

The National Institute of Standards and Technology (NIST) has provided a high-acceptable statistical tests algorithm for specifically evaluate the randomness of binary sequences. In this paper, the widely-used NIST test suite from NIST SP800-22 [**?**] is utilized with typical 1,000,000 random binary sequences. The test suite comprises 15 test methods which imply the random characteristic of the sequences. Where the robustness of the perfect randomness is described by P-values (probability values), for example, a P-values greater than a level of 0.01 suggests that the tested sequences is performing the random behavior with 99% of confidential level. In the case of multiple random sequences, the acceptable proportion of passing sequences can be defined as follows

$$(1-\alpha) \pm 3\sqrt{\frac{\alpha\,(1-\alpha)}{k}} \tag{2.18}$$

where α and k are the acceptable level of P-values and number of tested sequences, respectively. Table 2.2 summarizes the NIST test results of 1,000,000 binary sequences of 30 proportions, obtained from the proposed system. It can be clearly seen that the proportion of all testing methods are fall within the region of acceptable proportions (0.9355 – 1.044). Moreover, the P-values of overall testing methods were passed the acceptable level ($\alpha = 0.01$), which implies that the proposed system is a potential to use as the truly random number generator.

2.4.3 TestU01 Empirical Test Suite

TestU01 is an empirical randomness testing for RNG, based on software library. The TestU01 library consists of several statistical tests batteries, which is designed to search the non-randomness region of the test sequences, described by a P-value. The interval $[0.001 - 0.999]$ of P-value represent the passing level of the test sequences. In this paper, Rabbit and Alphabit batteries were utilized, include 26 and 9 subtests, respectively. Table 2.3 and Table 2.4 conclude the testing results of 220 binary sequences with 30 proportions, generated by the proposed system. Most of proportions can pass all the tests of Rabbit and Alphabit batteries.

Table 2.4 Summary of Rabbit battery.

Test Methods	**Parameter**	**Proportions**
smultin_MultinomialBitsOver		28/30
snpair_ClosePairsBitMatch	t=2	30/30
	t=4	30/30
svaria_AppearanceSpacings		30/30
scomp_LinearComp		30/30
scomp_LempelZiv		30/30
sspectral_Fourier1		30/30
sspectral_Fourier3		30/30
sstring_LongestHeadRun		30/30
sstring_PeriodsInStrings		30/30
sstring_HammingWeight	L=32	30/30
sstring_HammingCorr	L=32	30/30
	L=64	30/30
	L=128	30/30
sstring_HammingIndep	L=16	30/30
	L=32	29/30
	L=64	30/30
sstring_AutoCor	d=1	30/30
	d=2	30/30
sstring_Run		30/30
smarsa_MatrixRank	L=32	30/30
swalk_RandomWalk1	L=128	30/30
	L=1024	29/30
	L=10016	30/30

Table 2.5 Summary of significant performances and comparison to previous works.

	References	Types	CMOS (nm)	ADC	Entropy Source	Area (mm^2)	Power (mW)	Throughput (Mbit/s)	Energy (pJ/bit)
Non-ADC-Based	Yang *et al.* 2014, [[6]]	True	65	-	Jitter Accumulation	0.00038	0.54	23.16	23.31
	Kim *et al.* 2017, [[7]]	True	65	-	Jitter Accumulation	0.00092	0.29	8.2	32.61
	Kuan *et al.* 2014, [[8]]	True	40	-	Metastability	0.0014	0.0002	0.5	0.4
	Tokunaga *et al.* 2008, [[37]]	True	130	-	Metastability	0.145	1	0.04	25,000
	Brederlow *et al.* 2006, [[38]]	True	120	-	Noise-based	0.009	0.05	0.2	250
ADC-Based	Petrie *et al.* 2000, [[9]]	Pseudo	200	Algorithmic	Noise-based	1.5	3.9	1.4	2,786
	Callegari *et al.* 2005, [[41]]	Pseudo	-	Pipeline	DT-Chaos	-	-	10	-
	Pareschi *et al.* 2010, [[39]]	True	180	Pipeline	DT-Chaos	0.126	22	10	2,200
	Figliolia *et al.* 2016, [[10]]	True	55	$\Delta\Sigma$	Noise-based	0.0022	0.01	25	0.4
	Kim *et al.* 2017, [[40]]	True	180	SAR	DT-Chaos	0.21	0.000082	0.27	0.3
	This Work	**True**	**180**	$\Delta\Sigma$	**CT-Chaos**	**0.037**	**1.32**	**50**	**26.4**

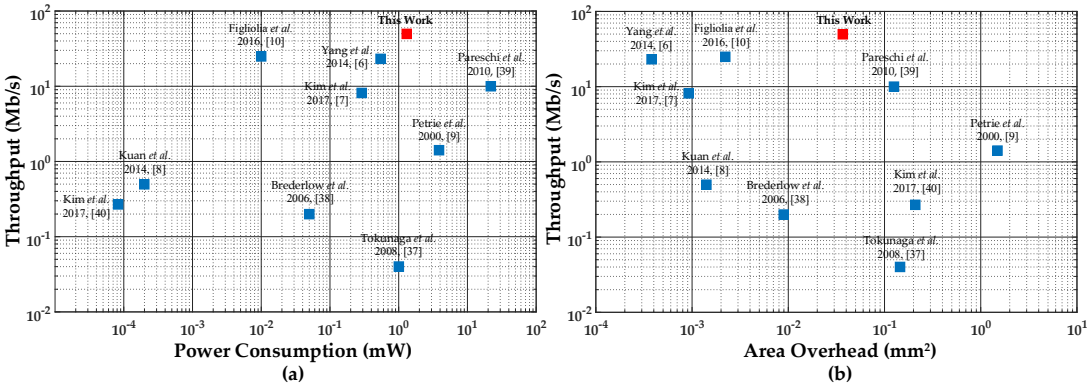

Fig. 2.17 Comparison of normalized throughput versus (a) power consumption and (b) total area with previous works.

2.4.4 Performances Measurement Results

The proposed TRBG is fully implemented in 0.18-μm CMOS standard technology with 1.8V single supply and total area overhead of 0.0376 mm^2. The maximum throughput is 50Mb/s at 1.32mW of total power consumption which performs the true random property, confirmed by the statistical measurements. Table 2.5 summarized the performances of proposed TRBG with the comparison of CMOS-based previous works. Where Fig. 2.17 depicts the energy-efficiency of proposed TRBG in term of throughput versus power consumption (Fig. 2.17(a)) and area overhead (Fig. 2.17(b)) compared with the previous works. It can be considered that the proposed TRBG has achieved the high-throughput topology with reasonable power consumption and area overhead. The results of energy-efficiency also suggested that the proposed TRBG has potentially offered to a fully embedded data encryption in high-security applications.

2.5 Bist Technique based on Chaotic Stimulus

There are many techniques for the mixed-signal testing depending on specialized approaches. Owing to the very large variations in property, structure and performance,

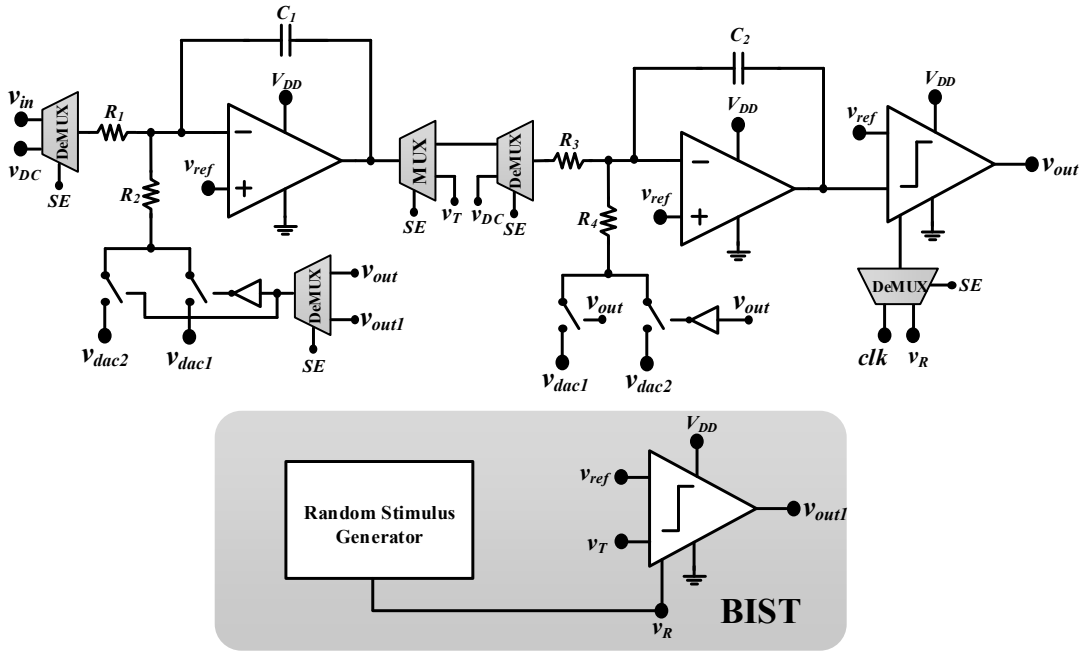

Fig. 2.18 Circuit diagram of the proposed BIST system.

designing the testing method is challenge, especially in analog circuits. Stimulus generation is an effective model that can extract most of faults characteristic, i.e. catastrophic and parametric faults. Faults signature is typically defined in order to distinguish between fault-free and faulty circuits which are suitable for sortable circuits in digital part. However, faults observation can be simply achieved by comparing signals of two symmetrical circuits without storage devices. For this reason, this approach emphasizes on the second-order model of the modulator, which relatively contains two symmetrical circuits. The major issues are introduced as following: (i) Simplify the faults observation method. (ii) Increasing faults coverage including catastrophic and parametric faults.

Consequently, the second-order $\Delta\Sigma$ modulator that described in previous section is utilized as circuit-under-test (CUT). Fig. 2.18 illustrates the circuit diagram of the proposed BIST system, involving random stimulus generator and additional dynamic comparator which absolutely identical used in the CUT. Five multiplexers are inserted

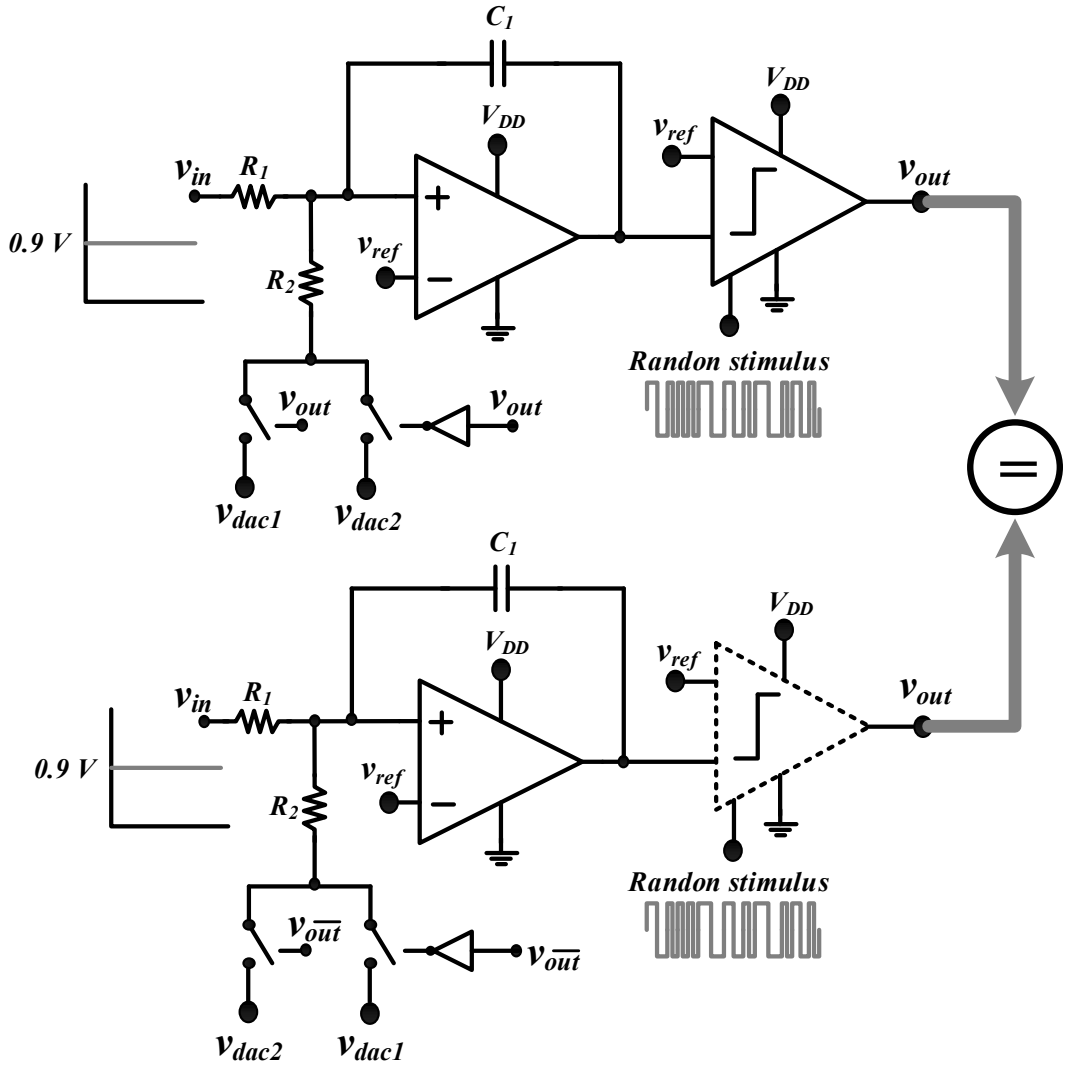

Fig. 2.19 The separated CUT in the test mode.

for separating the CUT into two circuits. Test operation can be selected by node SE in term of logic signal. The CUT is operated as generally designed in the normal mode. In the test mode, the CUT is separately performed similar to the first-order circuits as shown in Fig. 2.19. The input and clock sampling of each circuit are connected to DC reference voltage and the random stimulus generator, respectively. Due to the similarity of two separated CUTs circuitry, the output of each circuit supposed to be identical when the CUT is fault-free circuit. For this reason, fault detection can be simply achieved by observation the dissimilarity between two outputs of separated CUT.

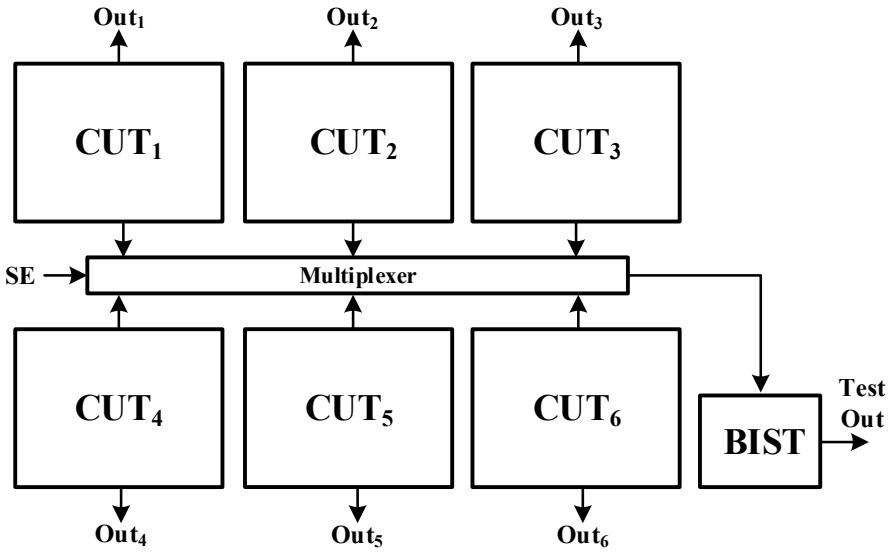

Fig. 2.20 Overall BIST system with multi-CUTs.

2.5.1 Experimental Results

The proposed BIST system was fully implemented through the Rohm 0.18 μm CMOS technology. Fig. 2.20 illustrates the block diagram of the multi-circuit testing demonstration. Six CUTs with BIST circuitry which designed corresponding to Fig. 2.18 were included for demonstrating different fault models. The CUT1 represents a fault-free circuit employed as a reference. Other five CUTs including CUT2-CUT5 were injected the different fault types as follows; Gate-Drain-Short (GDS) at M_1 Drain-Source-Short (DSS) at M_5, 10% deviation at C_c (refers to Fig. 2.10), 10% deviation at R_1 and 10% deviation at C_2 (refers to Fig. 2.9), respectively. The observations of test responses of six CUTs are exhibited in Fig. 2.21. As described in previous section, the faulty circuit can be detected by the dissimilarity between two output responses. It is clearly appearance in Fig. 2.21(a) that the output testing response of two nodes is totally equality in the CUT1 (fault-free circuit). On the other hands, catastrophic faults cause a massive error on testing responses of CUT2 and CUT3, which can be obviously detected in Fig. 2.21(b) and Fig. 2.21(c). Moreover, the capable of parametric faults

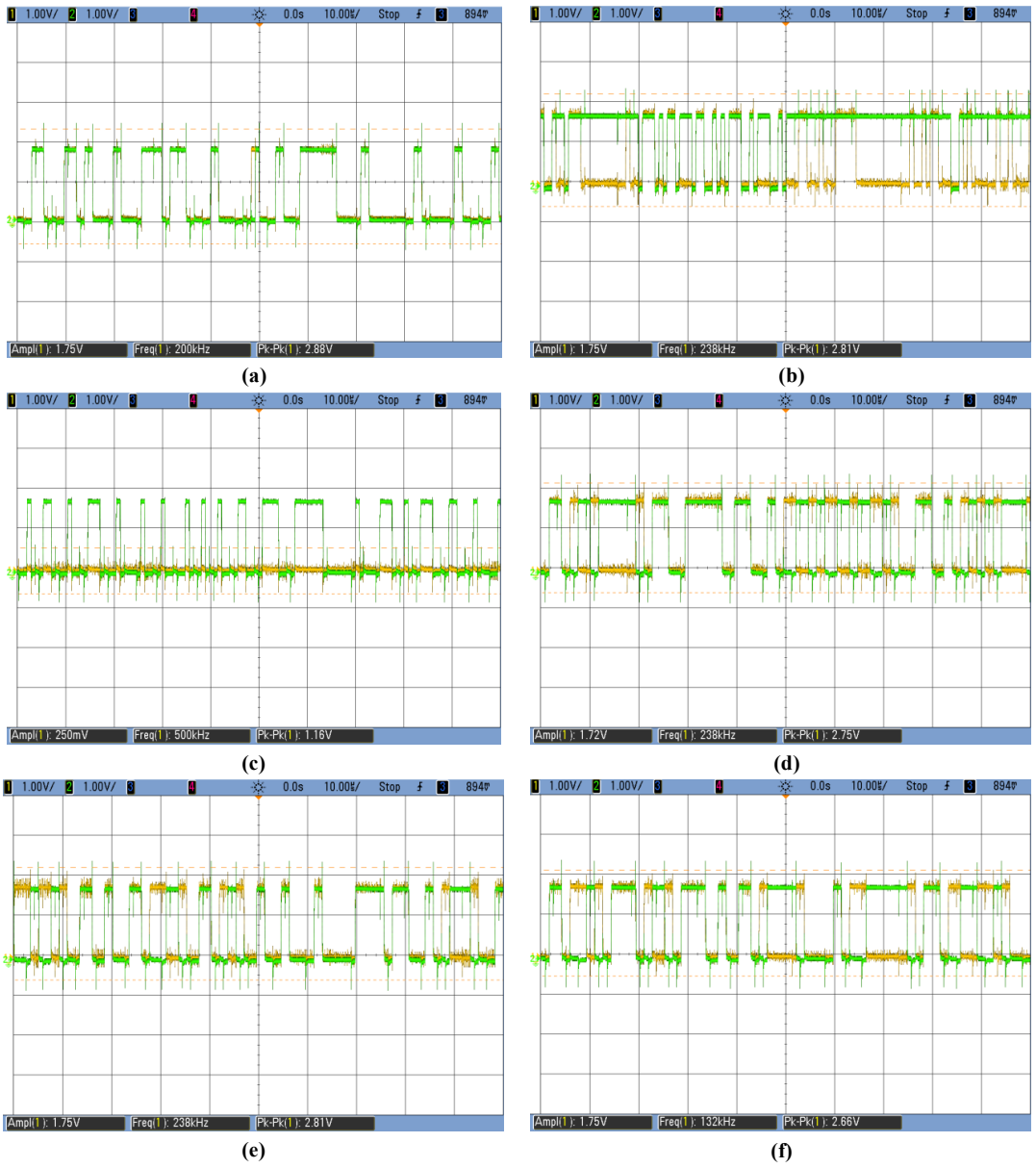

Fig. 2.21 Comparison between two outputs testing response from (a) CUT1, (b) CUT2, (c) CUT3, (d) CUT4, (e) CUT5 and (f) CUT6.

detection is also illustrated in Fig. 2.21(d), Fig. 2.21(e) and Fig. 2.21(f). It can be seen that even small deviation in parameter value, the dissimilarities of two testing response still occurred. Consequently, the concept of realizing the chaotic testing stimulus is acceptable for fault detection as the all faults injected are detected. The fault injection details and fault detection performances of proposed BIST system are concluded in

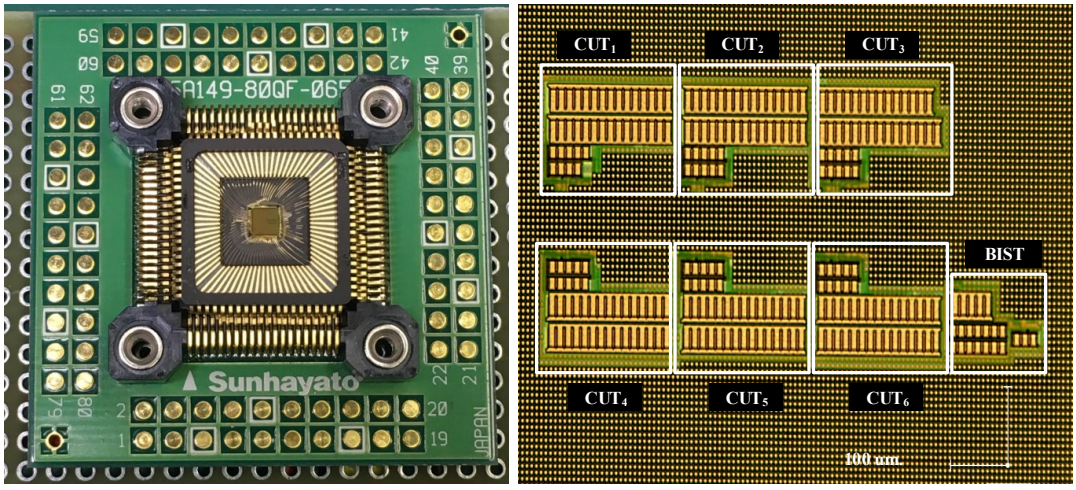

Fig. 2.22 Chip micro-photograph of the overall system with area of 0.294 mm^2

Table 2.6 Summary Performances of the Proposed BIST.

Circuits	**Fault Types**	**Details**	**Detected**
CUT1	Fault-free	-	-
CUT2	Catastrophic	GDS	Yes
CUT3	Catastrophic	DSS	Yes
CUT4	Parametric	10% deviation in C	Yes
CUT5	Parametric	10% deviation in R	Yes
CUT6	Parametric	10% deviation in C	Yes

Table 2.6. The chip micro-photograph of overall system is also illustrated in Fig. 2.22.

2.6 Conclusion

The design of a fully-on-chip true-random bit generator has been presented. The chaotic jerk oscillator is employed as an entropy source that provides a robust, a smoothly balanced-to-unbalanced adjustable of double-scroll attractors, and highly phenomenon of chaotic signals, investigated by qualitative and numerical analysis. The continuous-time 2^{nd}-order $\Delta\Sigma$ modulator with feed-forward topology is implemented as a mixed-signal interface in order to enhance the throughput of random bit sequences.

The TRBG property is evaluated by the widely-acceptable statistical methods, i.e. cross-correlation, autocorrelation, NIST SP800-22, and TestU01. The generated random sequences have passed all the statistical tests of NIST without any correlation either interim or inside the sequences, indicated by extremely low value of correlation coefficient. At the nominal supply voltage, the TRBG has achieved higher throughput with reasonably power consumption and area overhead than previously reported works. Finally, the widely-used structure of the second-order $\Delta\Sigma$ modulator has been used employed as the circuit-under-test. The modulator was divided into two first-order circuits and executed the chaotic stimulus when the test mode is operated. Faulty circuits have been verified through dissimilarity signals between two divided circuits. Demonstrations of the six different fault types which containing a fault-free, two catastrophic and three parametric faulty circuits have shown the capable to detect all injected faults. This technique eliminates the need of high-precision stimulus generation and simplifies complex faults characterization. The overall system has been fully fabricated on 0.18 μm CMOS standard technology without any digital processing units. Furthermore, this work has offered a potential alternative for non-intrusiveness BIST with high-speed testing approach in mixed-signal systems.

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Chapter 3

A Design-for-Structural-Testability for Simple Faults Detection in Analog $\Delta\Sigma$ Modulator

Data conversion between analog and digital signals is an important function in many electronic systems. This interface is basically performed by an analog-to-digital converter (ADC), which consists of a modulator and a digital filter as the analog and digital part, respectively. The Delta-Sigma ($\Delta\Sigma$) conversion technique has attracted attention since it was first introduced [1]. This technique provides both high dynamic range and allows high resolution conversion of low bandwidth signals, which are commercially used in many applications, such as high-precision measurement devices and multimedia systems. Due to the increasing demand for high resolution in audio/video quality, the complexity of the $\Delta\Sigma$ ADC is rising every year. Testing such a high precision ADC, especially its analog component, has become a challenge.

This chapter presents an alternative topology of structural-based testing for the discrete-time $\Delta\Sigma$ modulator. The proposed circuits can achieve the self-testable operation through the structural reconfiguration technique, while fault detection is performed

entirely on chip by the simple digital circuits.

3.1 Review on Design-for-Testability in the ΔΣ Modulator

Design-for-testability (DFT) and built-in self-test (BIST) strategies are an appropriate option to achieve high faults coverage and reduce the testing cost. Several approaches have focused on specification-based testing by characterizing the dynamic parameters of the modulator e.g., direct current (DC)-offset, gain error, integral non-linearity (INL), and differential non-linearity (DNL). This method provides an accurate measurement but typically requires a high-precision test stimulus, such as a linear-ramp generator [2, 3], sinewave [4, 5, 6], and pseudo-random patterns [7, 8, 9], which is relatively difficult to generate on-chip. Consequently, a fully digital testing scheme has been extensively proposed in the last decade. In [10, 11], a ΔΣ modulator is designed to offer the digital test stimulus that is encoded with the sinewave. Thus, the modulator performances can be defined and the need for analog testing stimulus is eliminated, but generating a digital stimulus always requires additional digital parts, such as a shift-register and digital filter. In [12, 13], the characteristics of the ΔΣ modulator can be measured by a single-bit digital stimulus, which is simply generated by reconfiguring the switch-capacitor network as a digital-to-charge converter. Most of expand analog components can be reused in the test mode and do not affect the modulator performance in the normal mode, so such strategies offer several advantages, including low cost and small area overheads as well as high-speed testing. Regardless, a major drawback of the specification-based approaches is the need for a digital processing unit or output response analyzer in order to characterize pass/fail in the frequency domain.

Less common approaches, meanwhile, have considered defect-oriented testing, as

necessitated by manufacturing process failure. The BIST for a continuous-time $\Delta\Sigma$ modulator is proposed in [14, 15] through the use of a test pattern generator (TPG) as the testing stimulus. High fault coverage (98%) is achieved with simple test response observation, but only catastrophic faults are verified. Likewise, both catastrophic and parametric faults can be detected in [16, 17] by using the circuit reconfiguration technique. The underlying idea is that the circuit-under-test (CUT) can be transformed into the oscillator by applying slight modifications. Fault detection can be subsequently achieved by measuring the deviation of normalized oscillation frequency. Additionally, the schemes in [18, 19] have suggested a simple method to analyze the analog test responses, the comparator with different reference voltage being employed to detect the amplitude and phase deviation of sinusoidal signals and the faults signature then being stored in the counters. Major benefits of this method include its yielding to a tolerance in the output responses and achievement of the pass/fail decision entirely on chip through the built-in hardware, which is the motivation of this study.

3.2 Design-For-Structural-Testability (DFST)

The typical DFT concept is to search for ways to improve the testability of the circuits. In other words, additional components are applied that provide a CUT with more controllability and observability. The additional circuitry may affect the fabrication cost and testing time as well as the performance of the main circuits, so the design aim is to optimize these properties. Most studies have focused on DFT-based functional testing, but is difficult to analyze the test responses entirely on chip. In addition, the overall failure in design variables related to gain, setting time, and pole error, mainly due to defects in the transistor level finally cause a circuit structural mismatch.

In this section, a defect-oriented technique is emphasized, where the defects are

physically modeled in terms of catastrophic fault and parametric deviation for each component of the CUT. The circuit structure of the CUT is modified by adding supplementary components and a reconfiguration technique in order to offer widely testability properties, referred to as a DFST. Fig. 3.1 shows the demonstration of DFST for a single-loop 2^{nd}-order $\Delta\Sigma$ modulator with an additional feed-forward coefficient. The input-output relation of the modulator in the z-domain is given by

$$Y(z) = \frac{x(z)\left[a_1 H(z)^2 + a_2 H(z)\right] + Q(z)}{a_1 H(z)^2 + a_2 H(z) + 1} \tag{3.1}$$

where Q(z) is the z-transform of the quantization error. The signal and noise transfer function can be expressed as

$$STF(z) = \frac{(a_1 - a_2) z^{-2} + a_2 z^{-1}}{(a_1 - a_2 + 1) z^{-2} + (a_2 - 2) z^{-1} + 1} \tag{3.2}$$

$$NTF(z) = \frac{\left(1 - z^{-1}\right)^2}{(a_1 - a_2 + 1) z^{-2} + (a_2 - 2) z^{-1} + 1} \tag{3.3}$$

This model gains the advantage of the feed-forward topology, which lowers harmonic distortion and has a higher signal-to-noise ratio (SNR) than an ordinary model. Likewise, as is clearly seen in Fig. 3.1, the model is nearly symmetrical, so the structure can be reconfigured to obtain a symmetric model in order to contribute to controllability and observability in the test mode. Thus, the symmetric structure of the 1^{st}-order $\Delta\Sigma$ modulators can be performed by adding another feedback loop and placing each integrator with the input, where the feed-forward coefficients a_1 and a_2 can be set to either same or difference value. Fig. 3.2 shows the reconfigured model of Fig. 3.1 in the test operation. The two circuits utilize the quantizer simultaneously, thereby enabling each circuit to be validated separately and the test responses then compared. Consequently, the major issues of this topology are introduced as following:

1. The feed-forward structure provides many advantages, such as relaxing the requirement of output swing, high SNR, and low harmonic distortion [16].

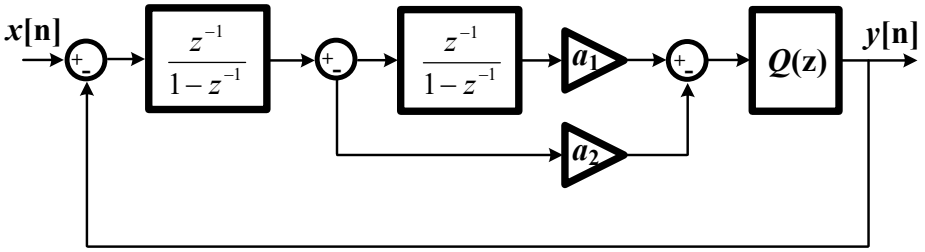

Fig. 3.1 Block diagram of the single-loop second-order $\Delta\Sigma$ modulator.

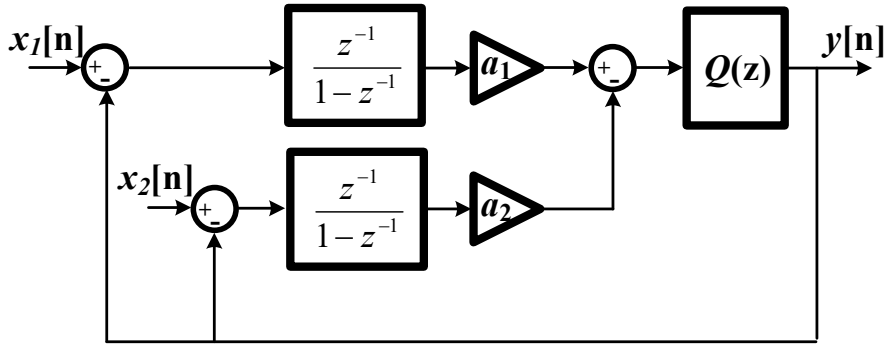

Fig. 3.2 Reconfigured model in the test condition.

2. The low need for additional components reduces the cost and area overheads in the test mode as well as decreasing the effect on the circuit performance.
3. Fault observation can be simplified with simple digital circuits, such as flip-flops and logic gates.

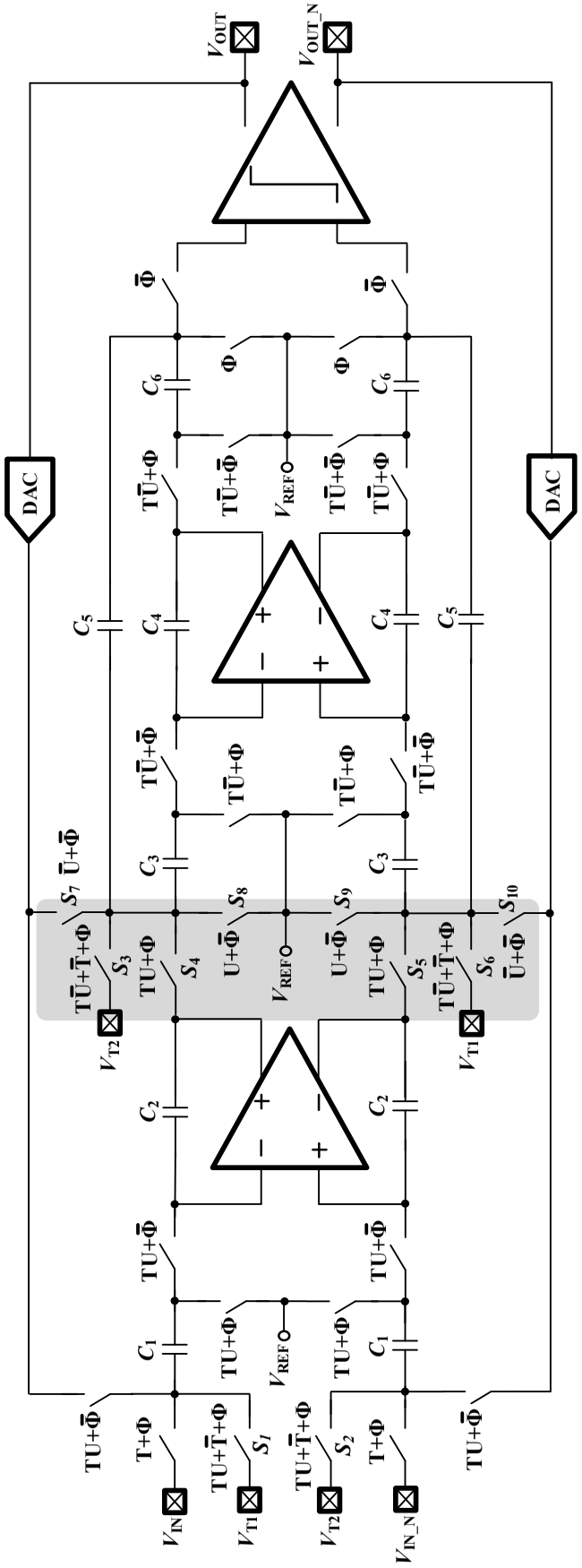

Fig. 3.3 Overall schematic of the proposed DFST $\Delta\Sigma$ modulator.

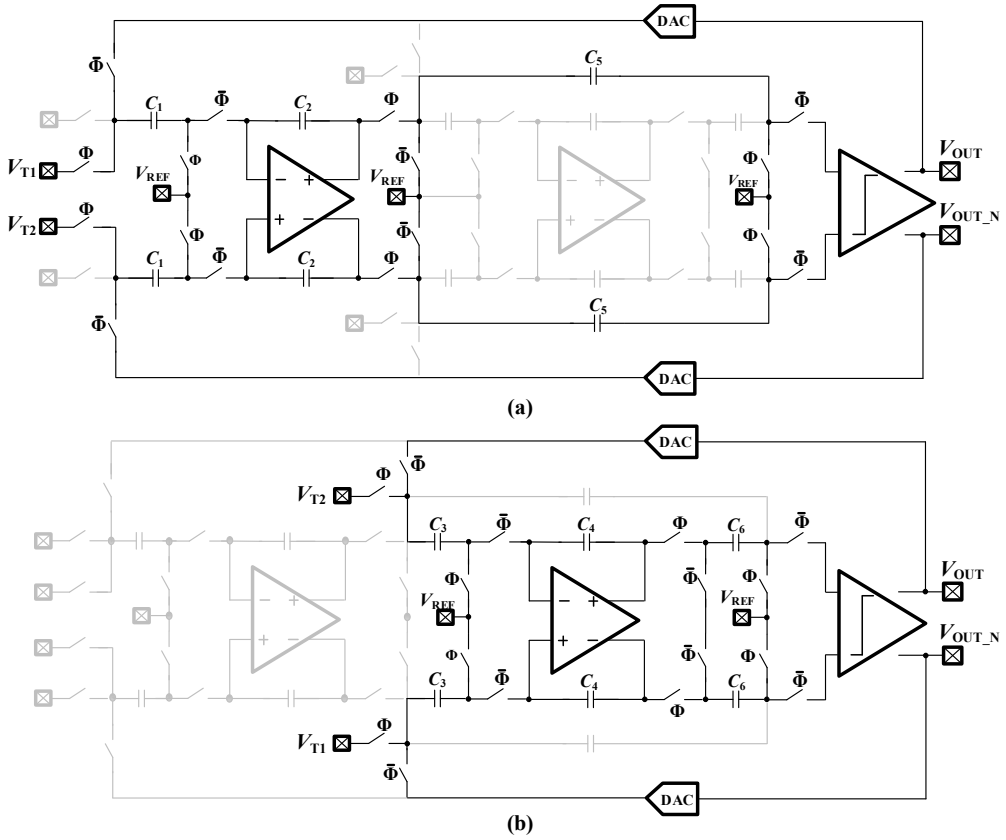

Fig. 3.4 The reconfigured modulator in test mode when the control signal U is set to 0 (a), and 1 (b).

3.3 Proposed DFST For Analog ΔΣ Modulator

3.3.1 DFST for the Second-order ΔΣ Modulator Architecture

A DFST is performed through a discrete-time structure. As most of the circuit components are based on switches, circuit reconfiguration can be simply done with low performance suffering. Fig. 3.3 illustrates the schematic of the single-bit second-order ΔΣ modulator with DFST technique. The proposed DFST modulator has two operation modes, normal and test, which are controlled by digital signal T, U, and basic logic gates. Note that the formula for the switches represents a Boolean expression. The ΔΣ modulator is executed as a single- loop with feed-forward topology where T and

U are fixed to 0. Switches S_1, S_2, S_3, S_6, and S_{10} are turned off, so the modulator is operated in the normal condition.

In the test mode, the ΔΣ modulator is divided into the symmetric first-order structure by the switches in the shaded area, while the DC inputs V_{T1} and V_{T2} are connected to each circuit. Afterward, the reconfigured modulators are individually evaluated by controlled signal U, where T is set to 1. Fig. 3.4 shows the reconfigured modulator in each phase of the test mode where U is set to 0 (4a) and 1 (4b). The thick lines represent the circuit area operated on. It is apparent that the reconfigured circuit is operated similarly to the first-order ΔΣ modulator, which employs the comparator together in both phases. The output of the modulator in z-transform can be written as

$$Y(z) = \frac{az^{-1}x(z) + \left(1 - z^{-1}\right) Q(z)}{(a-1)z^{-1} + 1} \tag{3.4}$$

where the feed-forward coefficient a can be defined by setting capacitor C_5 and C_6. Due to modulation, the difference of DC input levels, the output of the modulator is performed as the pulse waveform with fixed frequency. In addition, the DC inputs V_{T1} and V_{T2} are connected alternately in each phase of the test mode in order to characterize defects in the comparator. Therefore, the outputs of the two phases should be identical with inversion of 180° phases, due to the alternate connection of the DC input.

3.3.2 Faults Detection

The method that determines whether the circuit is fault-free or faulty is important for achieving the testability feature. The faults signature is typically defined in order to distinguish between a fault-free and faulty circuit according to what is suitable for storable circuits (a digital circuit). Pass/fail decisions in analog circuits are more cumbersome, however, due to tolerance bands in the specification margins. As mentioned, when the DFST ΔΣ modulator is operated in the test condition, it is evaluated

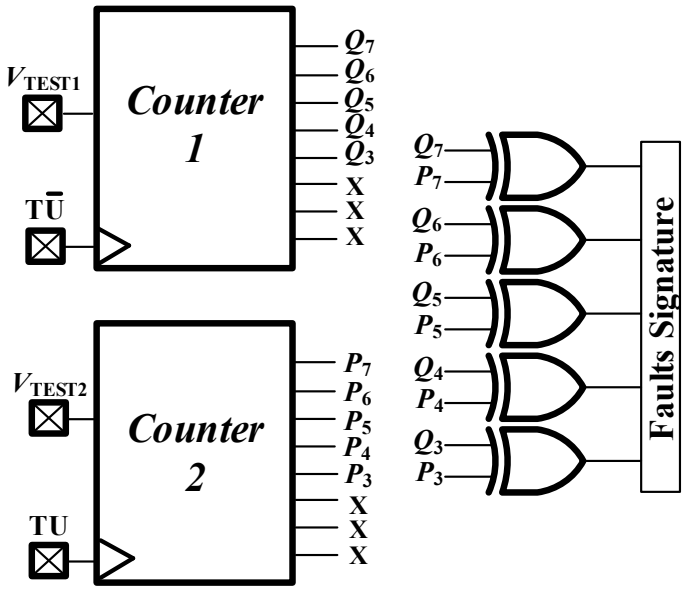

Fig. 3.5 The reconfigured modulator in test mode when the control signal U is set to 0 (a), and 1 (b).

separately, which generates the identical structure of two phases. For this reason, the simplest way to identify a faulty circuit is by observing the correlation of signal outputs in each phase. However, a small deviation may occur between the two outputs owing to the tolerance bands in analog components.

The simple pass/fail decision circuit is depicted in Fig. 3.5. The 8-bit counters are used in order to correct any fault signatures in reconfigured circuits, which are also controlled by signals T and U. This technique offers allowable tolerance bands for the three least significant bits, which are considered "don't care" bits. Consequently, the pass/fail circuit can be simply declared by comparing the other bits (bits 5-7) with basic logic gates. Otherwise, the large defect will cause an extreme deviation of frequency between the two reconfigured circuits and the counter values (while attainment of the same values in the two counters shows the system to be fault-free).

3.4 Overall Circuits Design

3.4.1 Operational Amplifier

The operational transconductance amplifier (OTA) is the core component whose implementation determines the performance of the $\Delta\Sigma$ modulator. Basically, the dominant specifications that affect the modulator performance comprise the bandwidth, speed, and stability, where a 60dB DC gain is adequate. A two-stage OTA is commonly used with Miller compensation. This can provide a high speed and high output swing but suffers from a poor power-supply rejection ratio (PSRR) and high power consumption. Another drawback is a difficulty in detecting parametric faults, which is due to the internal compensation components (e.g., resistor and capacitor). These limited performances can be compensated for by a folded-cascode OTA, which offers good input common-range, self-compensation, and high DC gain. In order to demonstrate the DFST configuration, a high-performance, class B, folded-cascode OTA is utilized as illustrated in Fig. 3.6(a). The differential-output DC gain and the power dissipation can be expressed as

$$A_{dc} = \beta\,(1+\lambda)\,(g_{mN} r_{dsN})^2 \tag{3.5}$$

$$P_{diss} = (I_{17} + I_{18} + I_{19} + I_{20} + I_{21} + I_{22})\,(V_{DD} + |V_{SS}|) \tag{3.6}$$

where β and λ are the relative values of N/P-transistors transconductance and the current flows in M_8, respectively. Table 3.1 summarizes the performances of the OTA.

3.4.2 Dynamic Comparator

The comparator is the secondary major component that affects the modulator performance. The requirements of this block are flexible, since the performance of the modulator is nearly insensitive to the comparator offset and hysteresis function. The

Table 3.1 Summary performances of the OTA

Performances	**Vaules**	**Units**
DC gain	75	dB
Unity-gain bandwidth	30	MHz
Phase margin	83	degree
Slew rate	30	V/µsec
Power consumption	115.43	µW

Table 3.2 Transistor aspect ratio of the designed modulator

MOS Transistors		**Aspect Ratio (W/L)**
Op-Amp	M_1-M_8	160
	M_9-M_{12}	40
	M_{13}-M_{20}	80
	M_{21}-M_{22}	20
Comparator	M_1-M_4	8
	M_5	12
	M_6-M_7	4
	M_8-M_9	12
	M_{10}-M_{11}	4
	M_{12}-M_{13}	4

dynamic comparator with SR latch is considered as a single-bit quantizer, as shown in the Fig. 3.6(b) schematic. In order to achieve low power and high speed, the circuit structure is designed based on Rahman *et al.* [20]. In this topology, the transistors M_5-M_{13} represent a latch circuitry, and a cross-coupled pair is formed by transistors M_2 and M_3. The comparator has two operation stages. The first stage is performed when ϕ = "0", all transistors are cut-off region, and the outputs V_{ON} and V_{OP} are connected to the power supply V_{DD}. The second stage is performed when ϕ = "1", when the current source M_5 begins for biasing currents of transistors M_1-M_4. This comparator dissipates

Table 3.3 Summary performances of the ΔΣ Modulator

Performances	**Vaules**	**Units**
Power supply	1.8	V
Input frequency	2	KHz
Oversampling rate	128	-
Max. SNR	80	dB
ENOB	12.99	bits
Power dissipation	389.86	μW
Area overheads	0.133	mm^2

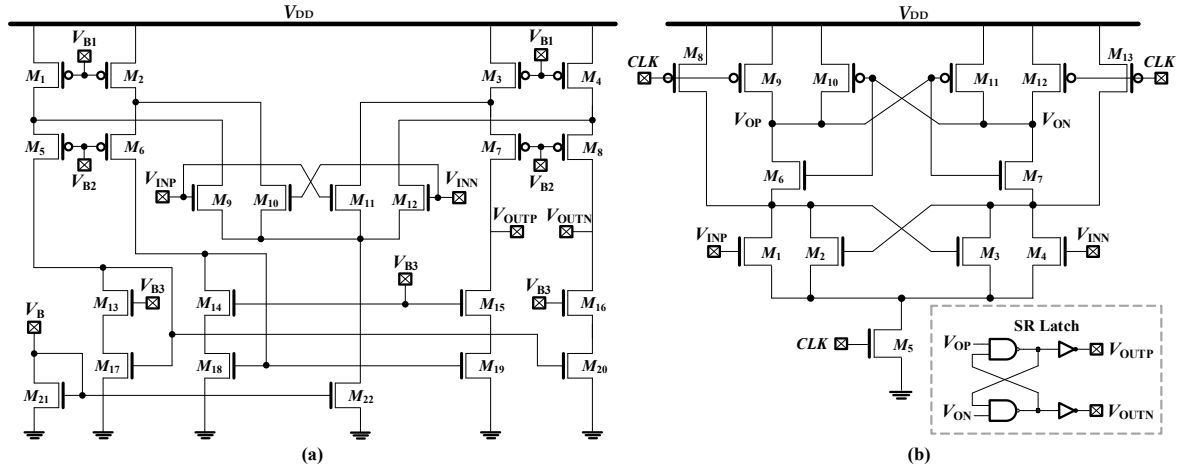

Fig. 3.6 Class B, fully-differential folded-cascode operational amplifier (a), and cross-coupled dynamic comparator with SR latch (b).

at approximately 150 μW with a 10-MHz clock frequency. The transistor aspect ratio of the overall sub-circuits is also shown in Table 3.2.

3.4.3 Modulator Performance

The performance of the proposed ΔΣ modulator was validated through a HSPICE environment operated in the ordinary condition. The 2 kHz-input sinusoide was used with a 128 over sampling ratio. The reference voltage V_{REF} was set as 0.9 V. Fig. 3.7 also

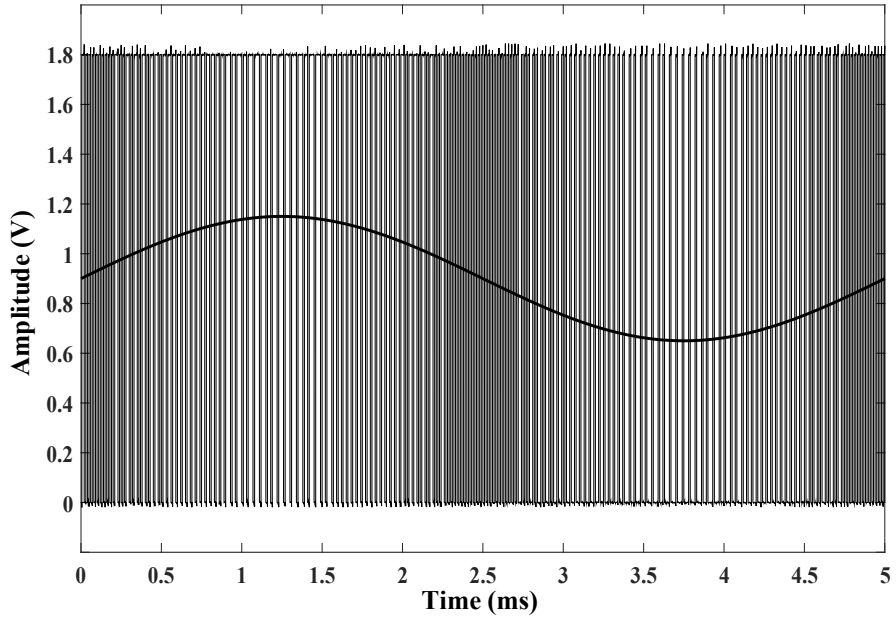

Fig. 3.7 Transient waveform of an input sinewave and modulated output.

shows the input sinewave and modulated output waveform in the time-domain. Fig. 3.8 exhibits the simulated power spectrum density (PSD) where a 32,768-point FFT with simple rectangular truncation window is employed. The measured maximum SNR was 80 dB and almost reached 13 bits of the effective number of bits (ENOB). Meanwhile, the overall power consumption as measured was less than 400 µW and dominated by the operational amplifier (115.43 µW). Table 3.3 summarizes the performances of the proposed $\Delta\Sigma$ modulator. It can be seen that the proposed $\Delta\Sigma$ modulator achieves the power efficiency and acceptable performances widely found in commercial applications.

3.5 Simulation Results

In this section, the proposed DFST $\Delta\Sigma$ modulator is operated in the test condition, with the symmetric feed-forward coefficient $a = 0.5$. The values of capacitors C_1-C_4 and C_5-C_6 set as 1 pF and 0.5 pF, respectively. The demonstration of fault observability is achieved through a 5 ms-transient analysis on the HSPICE simulation.

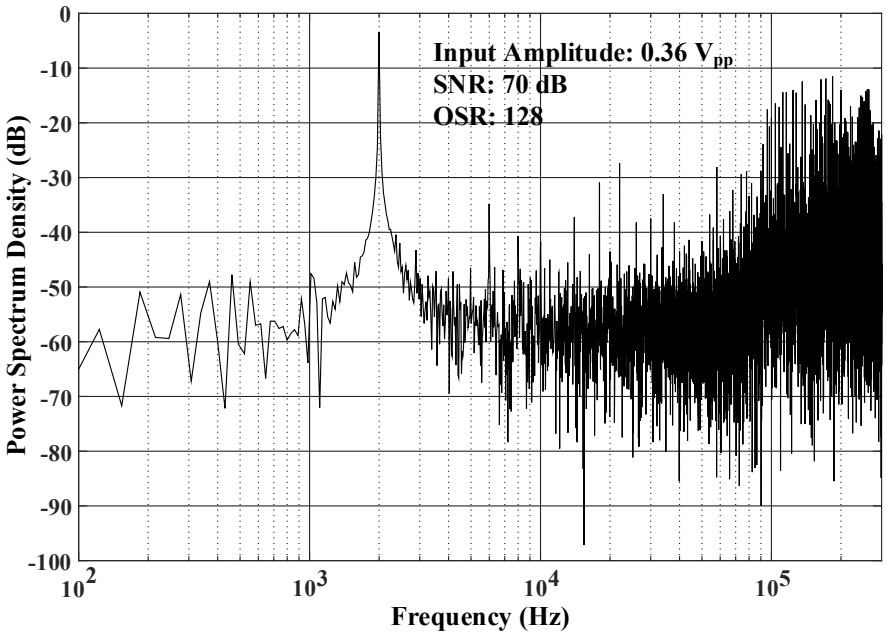

Fig. 3.8 Output power spectrum density of the proposed modulator.

3.5.1 Faults Models

In general, there is no standard faults model for analog circuits. However, fault modeling can be mostly realized at the transistor level by inserting resistors and a capacitor into the CUT. Here, different types of catastrophic faults were inserted, including short, open, gate-drain-short (GDS) and gate-open (GO). The short circuits represent bridging defects between two metal lines in an integrated circuit that can be simply modeled by a low resistance (R_S) connecting two bridge nodes. The open faults represent a line opening or thinning causing unconnected and floating inputs that is usually replaced by inserting a parallel combination of a large resistor (R_O) and a small capacitor (C_O) over possible signal paths. Note that the short and open defects were inserted on the connection lines, while GDS and GO were injected into sub-circuits of all the MOS transistors. In addition, all catastrophic faults injected on the switches and passive components were modeled based on approaches in [21-22].

Parametric faults occur due to small defects that are too minor to cause catas-

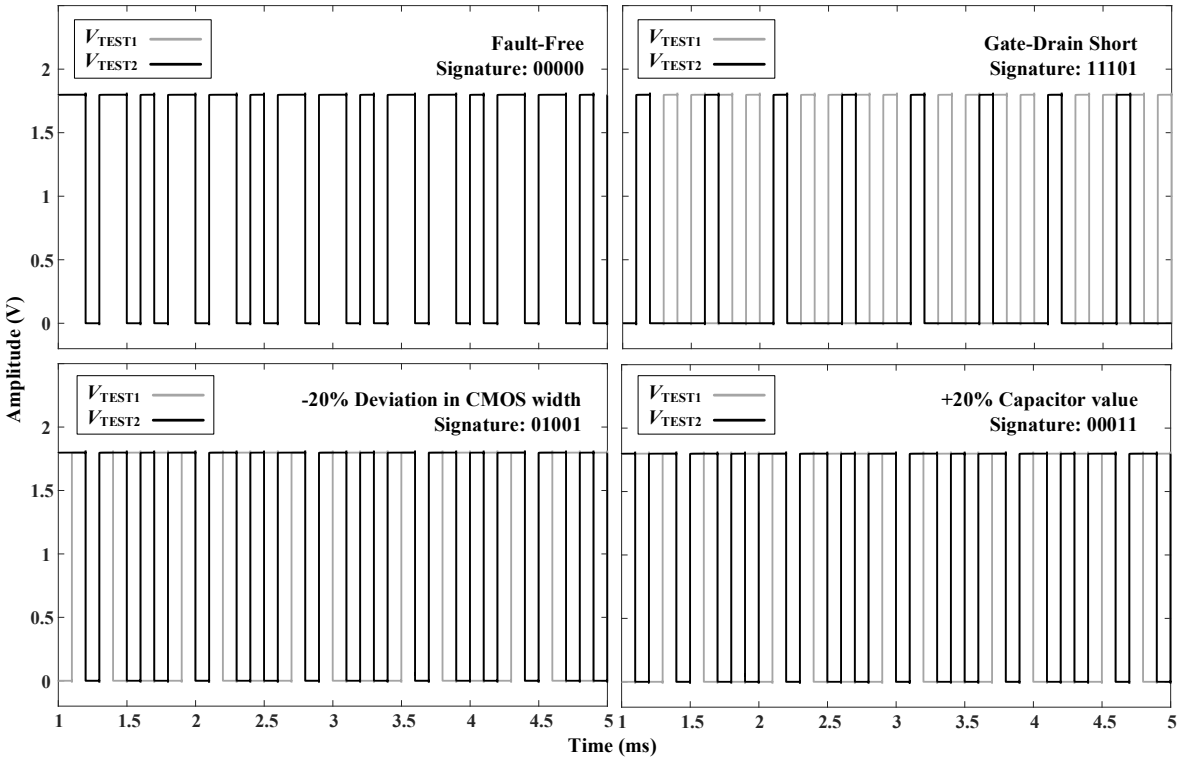

Fig. 3.9 Testing output response of four demonstrating CUTs.

trophic faults. This fault type causes the circuit parameters to deviate slightly from their designed values; the modeling of such characteristics is complicated, certainly at the physical level. Parametric fault modeling can be considered as based on a tolerance band acceptability method. In other words, the component parameters, such as resistor and capacitor values, are allowed to deviate in a small range due to behavior of the analog circuit, but large variations (e.g., $\pm 50\%$) are considered unacceptable. Furthermore, global parametric faults, such as gain, phase margin, and bandwidth deviation, directly impact on the system performance and will usually be detected in the production process. This topology realizes the deviation of each analog component involving transistor width and capacitor value variation. In order to ensure that all acceptable tolerance bands are distinguished with high yield coverage, the decision for acceptable range is based on specification violation. Thus, the fault tolerance band is determined

to ±20% in MOS transistor width and ±20% in capacitor values, which is implied by changing of the modulator SNR in the simulation.

Table 3.4 Summary of faults detectability of the DFST topology

Circuits	Fault Types	Details	Injected	Detected	Fault Coverage
Op-Amp 1	Catastrophic	Short	28	28	100%
	Catastrophic	Open	42	42	100%
	Catastrophic	GDS	22	19	86.36%
	Catastrophic	GO	22	20	90.90%
	Parametric	±20% deviation in width	44	35	79.55%
Op-Amp 2	Catastrophic	Short	28	28	100%
	Catastrophic	Open	42	42	100%
	Catastrophic	GDS	22	19	86.36%
	Catastrophic	GO	22	20	90.90%
	Parametric	±20% deviation in width	44	35	79.55%
Comparator	Catastrophic	Short	17	17	100%
	Catastrophic	Open	33	33	100%
	Catastrophic	GDS	13	12	92.30%
	Catastrophic	GO	13	13	100%
	Parametric	±20% deviation in width	26	22	84.62%
Modulator Top Level	Catastrophic	Short	14	14	100%
	Catastrophic	Open	42	42	100%
	Catastrophic	Switch short	34	34	100%
	Catastrophic	Switch open	34	34	100%
	Parametric	±20% deviation in C	24	16	66.67%
	Total		**554**	**527**	**92.86%**

Table 3.5 Comparisons of this work and other related topology

Characteristics	**Testing Topology**			
	Hu *et al.* 2008, [16]	Mozuelos *et al.* 2005, [25]	Chinazzo *et al.* 2017, [14]	**This work**
Technology	-	AMS 0.6-μm.	CMOS 0.13-μm.	CMOS 0.18-μm.
Results	Simulation	Simulation	Simulation	Simulation
Circuit-Under-Test	ADC.	Switched-Capacitor ADC.	Continuous-Time $\Delta\Sigma$ modulator	Discrete-Time $\Delta\Sigma$ modulator
Technique	Oscillation based reconfigured circuit.	Built-in charge sensor.	Test vector generation.	Circuit structural reconfiguration.
Faults Detection	Histogram testing.	Voltage charge observation.	Frequency observation.	On-chip faults signature observation.
External Test Equipment	Required	Required	Required	Not required
Catastrophic Faults	Detected	Detected	Detected	Detected
Parametric Faults	-	-	Detected	Detected
Faults Coverage	94.3%	96.46%	95.18%	92.86%

3.5.2 Testing Results

In the test condition, the proposed DFST $\Delta\Sigma$ modulator was reconfigured as described in Section 3. A set of catastrophic faults was modeled based on the realistic values mentioned previously, where R_S, R_O, and C_O were fixed as 100Ω, 10MΩ, and 1fF, respectively. A fault-free circuit was indicated by the relatively similarity (i.e., ±3) on the counter values. Fig. 3.9 shows the transient waveform of four CUTs in the test condition, including a fault-free circuit, GDS, -20% transistor width deviation, and +20% capacitor deviation. The solid and dashed lines represent the transient output when the signal U is set to 0 and 1 respectively. As expected, the output response of the fault-free circuit displayed relatively equality after two phases of the testing process; the obviously error between two testing outputs is shown at three faulty CUTs, yielding tremendous deviation in the counter value.

Table 3.4 summarizes the simulated results of the proposed system. It is apparent that those short and open faults injected into the signal paths were completely detected. This may due to the absolutely failure in the modulator operation, so the counters values were extremely different. The GDS and GO on the MOS transistors were also captured. displaying almost complete detectability; failures were undetected in a few transistors of the Op-Amp because only a small violation occurred on the overall circuit. For example, the GDS on transistor M_1 of the Op-Amp caused a short circuit between the V_{DD} and M_1 gate that did not greatly change the DC condition of the component.

In the case of parametric faults, the proposed DFST system also indicated observability. The fault coverage of transistor width deviation attained 80% in all sub-circuits. It is interesting to note that the worst faults coverage, of 66.67%, was revealed for capacitor value variation. This may imply that the frequency of the modulator with a DC input is relatively durable in respect of small capacitor value variation. Finally,

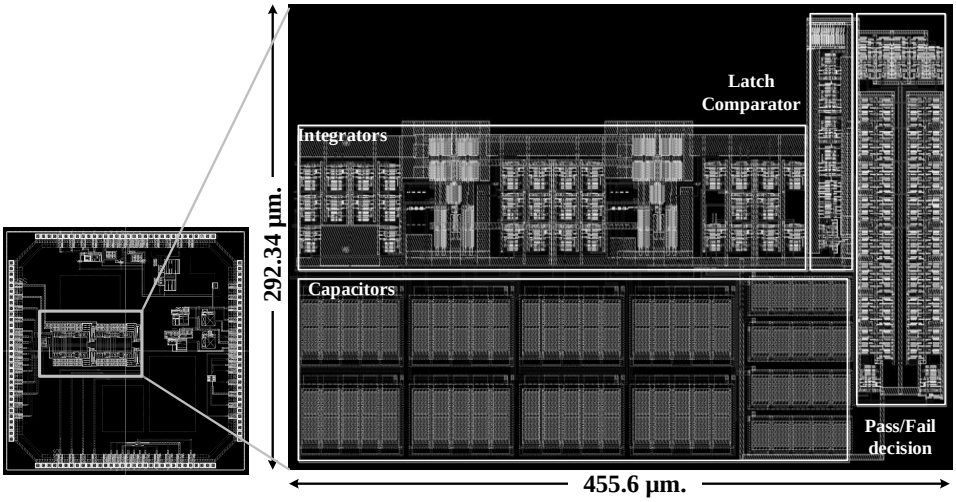

Fig. 3.10 Layout diagram of the proposed DFST $\Delta\Sigma$ modulator.

Table 3.5 summarizes the comparisons of this work to other design-for-test techniques. The built-in charge sensor technique, proposed by Mozuelos et al. (2005), has indicated the highest faults coverage (96.46%), However, only catastrophic faults were detected with an external test equipment. Although, either catastrophic or parametric faults can be detected by Chinazzo et al. (2017) with a test vector generation technique, faults models have been described ambiguously and long-time simulation (2.5 hours) is necessary. Likewise, this work introduces a built-in testing technique where external test equipment and data analyzer are not necessary. High fault coverage, including both catastrophic and parametric faults, can be detected, providing an on-chip pass/fail decision. Fig. 3.10 also shows the overall circuit layout diagram in 0.18-μm CMOS standard technology.

3.6 Conclusion

A design-for-structural-testability topology for the 2^{nd}-order $\Delta\Sigma$ modulator has been presented. A test operation can be achieved through the structural reconfiguration technique. In other words, circuit structure may be reconfigured and operated as

two symmetric circuits structure, thus verifying faulty circuits by the different output waveforms, which can be simply observed through faults signature, indicated by a digital counter circuit. Simulation of the modulator performance also implies the appropriate features with 80 dB for SNR at 128 OSR. Demonstrations of system testability indicated controllability and observability, with simulated test results at 92.86% of total coverage of faults involving catastrophic and parametric defects. This technique eliminates the need for high-precision stimulus generation and simplifies the fault characterization process.

3.7 Reference

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Chapter 4

Phase Difference Analysis Technique for Parametric Faults BIST in CMOS Analog Circuits

The BIST based on a phase difference analysis technique for the analog circuits is presented in this chapter. The test operation is achieved through the detection of phase shifting between two signals (i.e. the circuit-under-test and the reference clock). The faults signature is simply generated, and diagnosed by digital circuits, including a counter and basic logic components. The test stimulus generation and pass/fail decision are accomplished entirely on-chip, and also offers the range of tolerance in the passive analog components with eliminating the need for the external test equipment.

4.1 Review on Parametric Faults Detection in Analog Circuits

Analog circuits are the interface between natural signals and the digital processing. This role has rapidly gained a significance due to the need for high accuracy sensors and converters in modern systems. Nowadays, the nanometer-scale technology brings

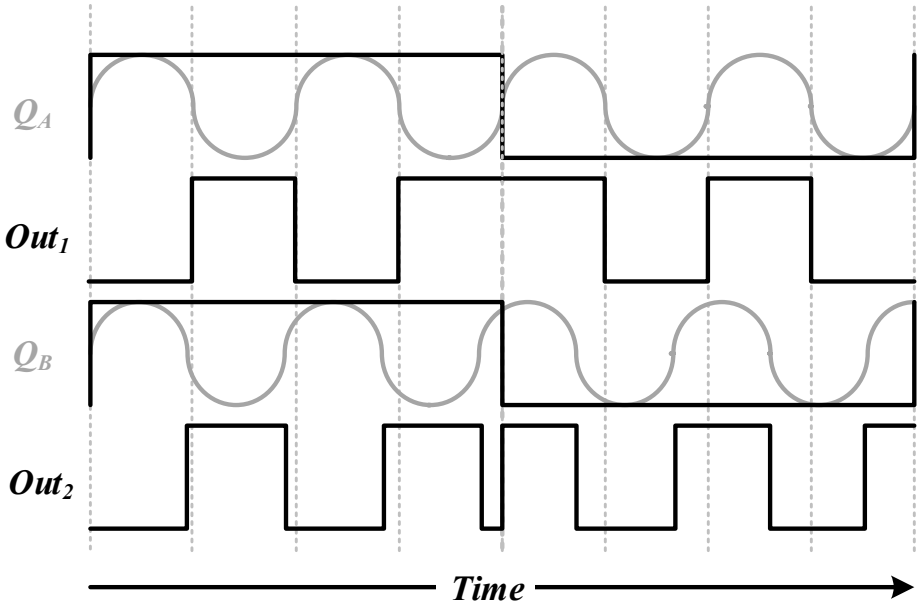

Fig. 4.1 Generation of faults signature using phase difference technique.

the feasibility of integrating analog circuits together with digital circuits into the same chip. The integration density is rapidly increased as well as the complexity of circuits, resulting in the greater demand for a suitable testing strategy. However, testing such a system is cumbersome especially, in the analog part. Owing to the very large variations in property, structure, and performance, designing the analog testing methods become a challenge. Moreover, characterization of the parametric deviations is difficult due to the allowable of the tolerance bands in the specification margins. Therefore, testing methods of the analog circuits are costly, time-consuming and may encounter issue of reduced performance due to the introduction of additional circuit components.

Built-In Self-Test (BIST) received considerable attention as a means of reducing testing time while also eliminating the need for costly and time-consuming from using external test equipment. Several BIST techniques for analog and digital circuits have been proposed in the last decade. Meanwhile, most of BIST techniques for the digital circuits are designed to be a fully on-chip, there is still less common approach for built-in testing hardware in analog circuits. Several approaches have focused on the

monitoring of circuits parameter such as amplitude [1, 2], current [3], and DC-offset error [4]. These methods provide an accurate measurement, however typically requires a high-precision test stimulus such as a linear-ramp generator [5], sinusoidal waveform [6] as well as pseudo-random patterns [7], which is relatively difficult to generate on-chip. In addition, detection the parametric variation is usually rather crucial. A fast-Fourier transformation (FFT) is used in [8] in order to analyze the circuit specifications error. High sensitivity for parametric deviation is the feature of this technique but requires an external response analyzer. Recently, an oscillation-based test (OBT) method is widely gained the attention in the analog and mixed-signal circuits. The underlying idea is to eliminate the need for external testing generation. In other words, the CUT can be transformed into the oscillator by applying slight modifications. Afterwards, the frequency characteristic is simply observed such as amplitude, a center frequency, and distortion. The oscillator-based BIST for the analog filters is proposed in [9, 10], the DC gain, ripple, and the cut-off frequency are measured with high faults coverage. However, the pass/fail decision is based on monitoring and observing technique. The hardware-based pass/fail decision for OBT is presented in [11, 12]. In this case, a simple comparator and counters are employed in order to convert the frequency into a number that represents a faults signature. Although, this technique achieves an on-chip pass/fail decision and contributes the tolerance bands in analog circuits, the small deviation in phase and frequency may lead to undetectable faults.

4.2 Phase Difference Analysis Technique

In general, there is no monotonic testing design for the analog circuits due to the large variation of the structure, performance, and specifications. The practical way is to search for methods that improve the observability of the testing process. Such

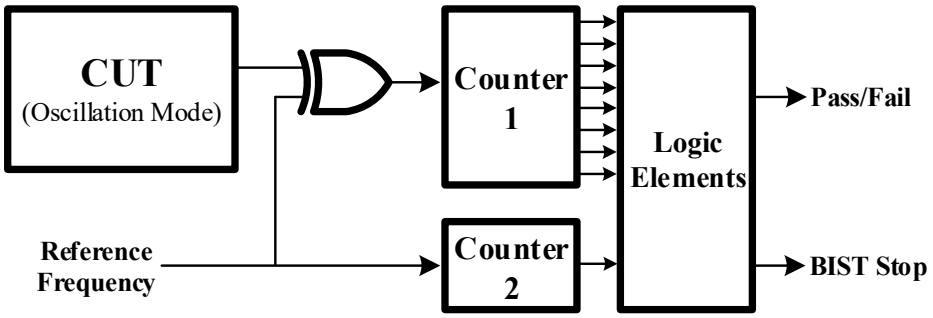

Fig. 4.2 Block diagram of the proposed system.

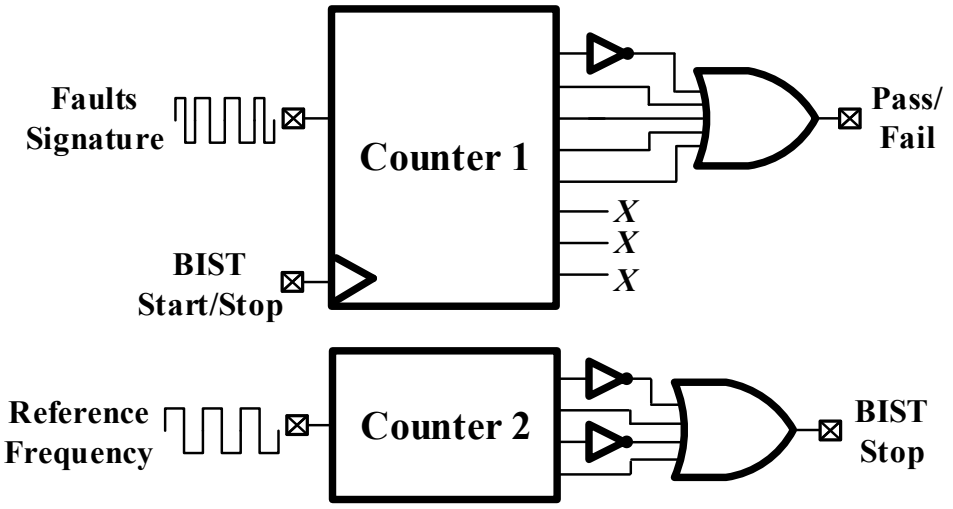

Fig. 4.3 Demonstration of the pass/fail decision circuit.

methods can be performed by BIST system, which the testing process can be modified depending on the features of a circuit-under-test (CUT). The main purpose of BIST is detecting all the possible faults in CUT for both catastrophic and parametric faults. Fig. 4.1 illustrates the demonstration of the faults signature generation using the phase difference detection. The signal Q_A and Q_B are compared by the reference clock signal. It can be clearly seen that even though these two signals are slight variation in frequency, the output responses are largely different. This feature reveals the sensitivity to the phase shifting, which cannot be occurred by the frequency or amplitude detection, and suitable for the BIST in oscillation system.

4.2.1 The Proposed Technique for the BIST

Fig. 4.2 depicts the block diagram of the proposed BIST technique. The system comprises a clock generator, two counters, the digital logic components and the Exclusive OR (XOR) gate as a basic phase detector circuit. Oscillation reconfiguration technique is used in order to transform the CUT into the oscillator in the test operation. Then, the phase shifting of the modified CUT and the reference clock is compared together by the XOR gate, which provides the signature for any circuits characteristic. The faults signature is subsequently accumulated by the digital counter 1 in the binary number format, which is typically characterized by the digital logic components. Additionally, the testing operation period can be determined by the digital counter 2 that stores the number of the reference clock pulse, therefore, the test response (Pass/Fail) of the system is exposed automatically.

4.2.2 Faults Detection

According to the previous section, due to the small deviation in parametric components values and the tolerance bands in the specification margins, pass/fail decision in analog circuits is relatively cumbersome. The method that determines whether the circuit is fault-free or faulty is important for achieving the testability feature. As mentioned, the small deviation of phase shifting between two signals can provide an identical output response as the faults signature. For this reason, the simplest way to identify the correlation of signature is by converting into the binary number format and comparing each bit in the same period. The on-chip pass/fail decision circuit is shown in Fig. 4.3 comprises two counters and the digital logic gates. While the 8-bit counters are used in order to transform the phase correlation into the binary number, another 4-bit counter determines test operation period, according to the amount of reference clock

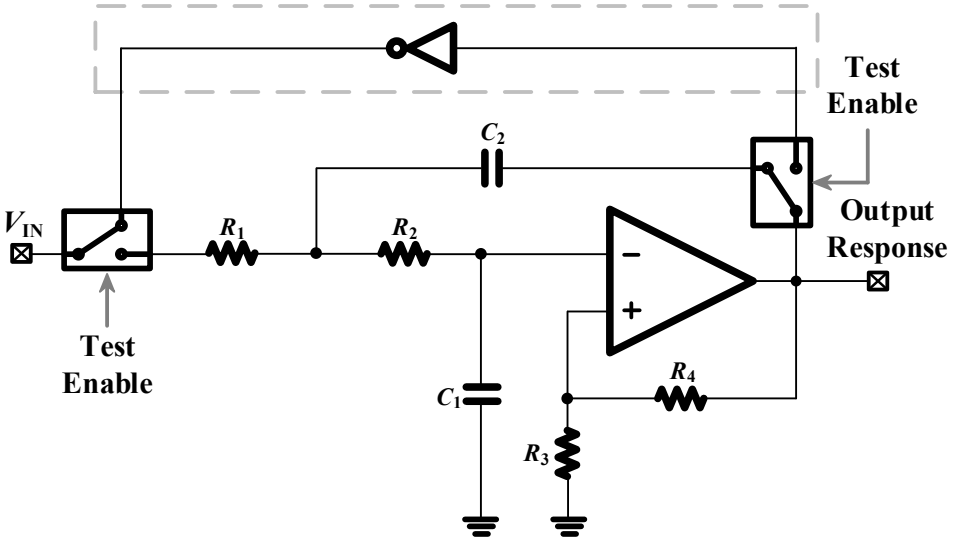

Fig. 4.4 Reconfigured model in the test condition.

pulses. Furthermore, this technique offers allowable tolerance bands, which indicates by *"don't care"* in the three least significant bits. Otherwise, the large correlation in phase shifting will cause the extremely difference number that indicates only on the most significant bits (5-7). For example, the 50 kHz clock reference and 2 ms testing time are defined, so the binary number in counter 2 implies "0101". In this period, the binary number in counter 1 will indicate the testing response and be compared to the fault-free signature, in this case is "01111XXX" (X means *"don't care"*).

4.3 The System Architecture

4.3.1 A Modified Sallen-Key Low Pass Filter as the Oscillator

In order to detect the phase variation, it is necessary to design the self-oscillation topology for the CUT. The Sallen-Key second-order active low-pass filter is utilized as illustrated in Fig. 4.4 The circuit is operated as its designed in the normal condition. In the test condition, the circuit is converted into the oscillator based on the Barkhausen

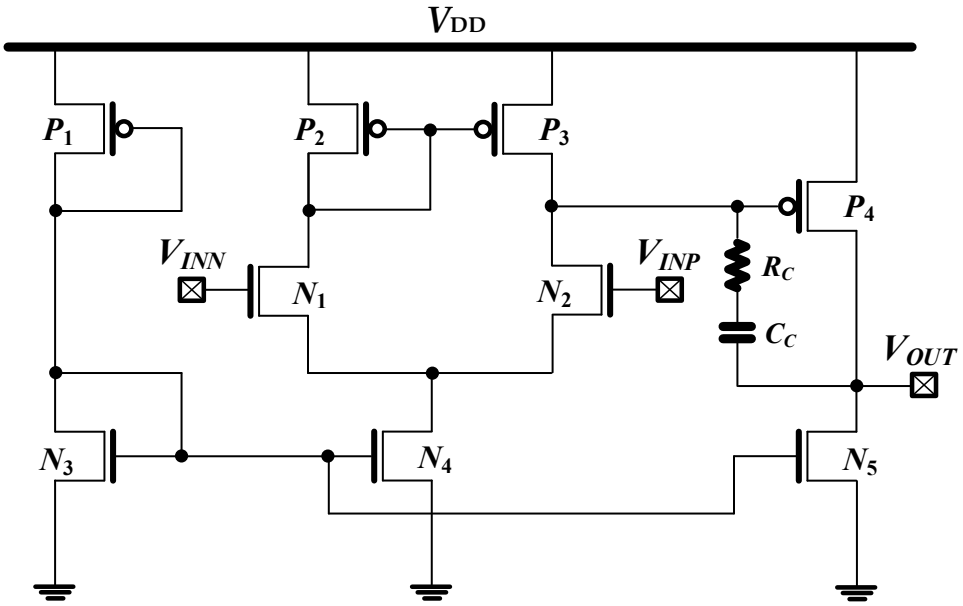

Fig. 4.5 The two-stage operational amplifier with RC compensation.

criterion as follows

$$|A(j\omega_0)\,H(j\omega_0)| = 1 \tag{4.1}$$

$$\angle A(j\omega_0) + \angle H(j\omega_0) = 0 \tag{4.2}$$

where $A(j\omega_0)$ and $H(j\omega_0)$ are the transfer function of the system and feedback loop, respectively. This criterion implies that the oscillation feature can occur if there are no attenuation and phase shift in the feedback system. For this reason, the additional inverter is applied in order to perform the feedback loop, represented in the shaded area. Note that, when the test operation is enabled, the filter is a self-oscillation system with 183 kHz frequency at the fault-free condition.

4.3.2 An Operational Amplifier

The two-stage operational amplifier (Op-Amp) with RC frequency compensation circuit is used for the low-pass filter. Fig. 3.5 depicts a schematic of the Op-Amp consists of a differential input stage represented by transistors N_1 and N_2, current mirror source represented by transistors P_2 and P_3, and a PMOS amplifying represented by transistors

Table 4.1 Transistor aspect ratio of the operational amplifier

MOS Transistors	**Aspect Ratio (W/L)**
N_1-N_2	60
N_3-N_4	30
N_5	180
P_1	30
P_2-P_3	40
P_4	45

P_4. This circuit is operated by single power supply V_{DD} and current source P_1. The required gain and bandwidth of the amplifier are defined by the simulation. The DC gain and power dissipation can be expressed as

$$A_V = \frac{2g_{mN2}g_{mP4}}{I_{N5}\left(\lambda_{N2}+\lambda_{P3}\right)\left(\lambda_{N5}+\lambda_{P4}\right)} \tag{4.3}$$

$$P_{diss} = \left(I_{N3}+I_{N4}+I_{N5}\right)\left(V_{DD}+|V_{SS}|\right) \tag{4.4}$$

where g_m and λ are the N/P-transconductance and channel length modulation of MOS transistors, respectively. In addition, simulation results from HSPICE software imply that the designed Op-Amp can achieve a unity gain bandwidth (GBW) more than 60 MHz with a load capacitance of 1 pF and phase margin of 57°. The DC gain of the Op-Amp is higher than 75 dB at 30 μA bias current and the measured power dissipation is approximately 190 μW. The transistor aspect ratio of the Op-Amp is also shown in Table 4.1.

4.4 Simulation Results

This section describes the simulation of testing results when the CUT is operated in the test mode. Several catastrophic faults were injected, including short, open, gate-drain-short (GDS) and gate-open (GO). While the short circuits can be realized as

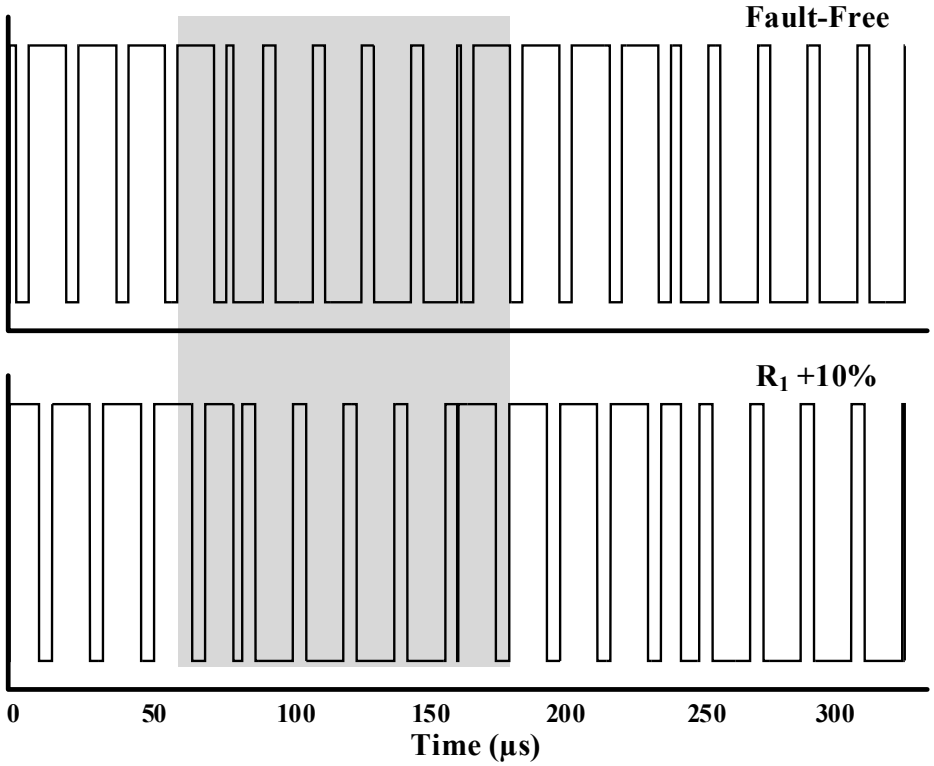

Fig. 4.6 The output waveform in transient between the fault-free and faulty circuit.

bridging defects between two metal lines in an integrated circuit that can be simply modeled by a low resistance connecting between nodes. The open defects represent a line opening and floating inputs, which is usually replaced by inserting a parallel combination of a large resistance and a small capacitor over the possible signal paths. The parametric faults are modeled by varying the components value based on the acceptable range for the specification violation. In this case, the fault tolerance band is determined to $\pm 20\%$ of the overall passive components. Fig. 4.6 shows the output waveform in transient of the fault-free and +10% resistor values of the faulty circuit. It is clearly seen that the small parameter deviation can produce the phase difference (shaded region), which lastly detected by the 8-bit binary number. The 20 kHz reference clock is employed and 0.8 ms of the test period is determined. At this period, the values of the counter indicate at 199 with two least significant bits, so the tolerance band of this system is in the range

Table 4.2 Summary of faults detectability of the proposed system

Circuits	**Fault Types**	**Details**	**Injected**	**Detected**	**Faults Coverage**
Op-Amp	CF	Short	10	10	100%
	CF	Open	10	10	100%
	CF	GDS	8	8	100%
	CF	GO	8	8	100%
Filter	CF	Short	6	6	100%
	CF	Open	6	6	100%
	PF	±20% Res.	8	7	87.5%
	PF	±20% Cap.	4	3	75%
Total			**60**	**58**	**96.67%**

CF = Catastrophic Fault, PF = Parametric Fault

Table 4.3 Summary of undetectable bands in the passive components.

Passive Components	**Undetectable Range**
R_1	-10% ∼ +5%
R_2	-20% ∼ +25%
R_3	-20% ∼ +10%
R_4	-5% ∼ +10%
C_1	-20% ∼ +25%
C_2	-10% ∼ +5%

of ±3 (i.e. "10001XX"). Table 4.2 summarizes the simulation results of the proposed technique. It is apparent that those catastrophic faults injected into the CUT were totally detected. This is caused by the extremely failure in the filter, which is clearly indicated by the counter. Most of the injected parametric faults were also captured (83.3%) with only two undetectable cases (R_2 and C_1). This may imply that these components are less sensitive to the phase and frequency of the system. In addition, the

Table 4.4 Comparison of the testing time.

	Conventional Technique	**[12]**	**This work.**
Time(ms)	1.0	2.4	0.8

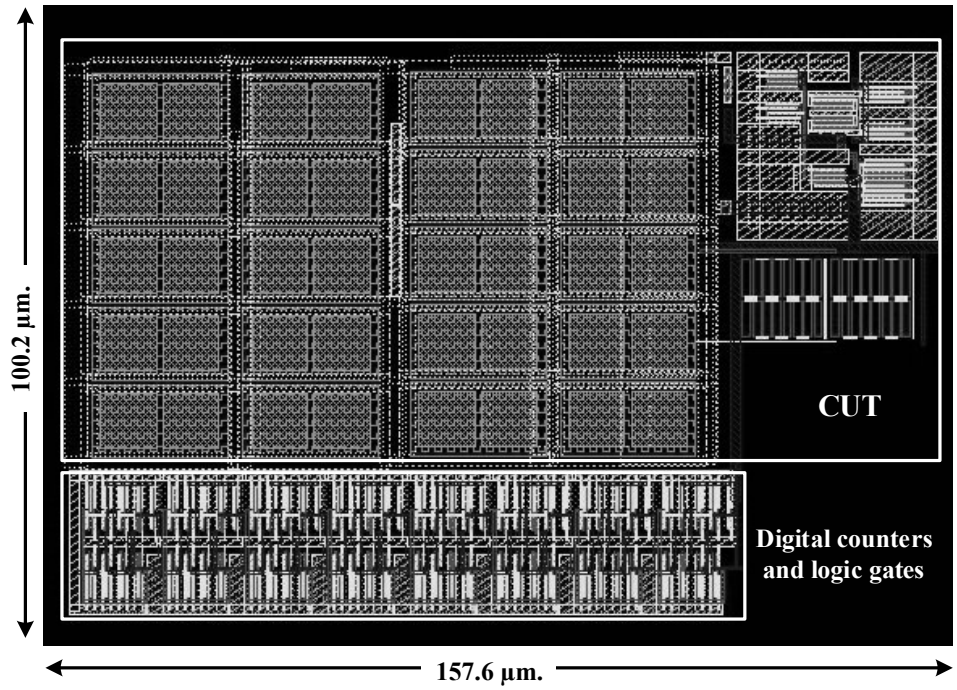

Fig. 4.7 The layout diagram of overall circuits in 0.18-μm CMOS technology.

undetectable tolerance band in the values of passive components was also evaluated, as summarized in Table 4.3. In order to reduce these tolerance bands, we suggest that the number/amounts of don't care bits should be reduced, while clock frequency and the testing time should be adjusted to the appropriate value. Fig. 4.7 also shows the overall circuit layout diagram in 0.18-μm standard technology.

4.5 Conclusion

The BIST based on a phase difference analysis technique for the analog circuits has been presented. The testing technique is based on the detection of phase shifting

between a reference clock signal and a modified circuit-under-test (CUT) as an oscillator, which is represented by the active Sallen-Key low pass filter. This technique has provided faults coverage of 96.67%, where all catastrophic fault of the CUT can be detected and the faults tolerance band of all passive components is determined to ±20%. The implemented BIST can eliminate the need for external test equipment by using a compact digital circuit which can be fully designed on-chip. This work has proposed a significantly high fault coverage and fully on-chip BIST technique for analog circuits as well as the potential of reducing the testing time as shown in Table 4.4.

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Chapter 5

BIST and Calibration Technique in Continuous-Time $\Delta\Sigma$ Modulator

This chapter presents a BIST method with self-calibration feature for the continuous-time $\delta\sigma$ modulator. The chapter initially reviews the conventional oscillation testing approaches, and calibration schemes in mixed-signal circuits. The simple circuitry such as a frequency-to-DC circuit, a windows comparator, and basic logic elements are utilized as the faults detection circuits. The calibration system is additionally implemented through the resistor array with a feedback network in order to adjust the gain value of the CUT. Simulation results show the capable of faults detection involves catastrophic and parametric variation. Moreover, the signals-to-noise ratio (SNR) of the CUT can be preserved at the acceptable level against the failure circuitry.

5.1 Reviews on $\Delta\Sigma$ Modulator with BIST and Calibration Technique

Table 5.1 summarizes tree related BIST and calibration techniques for the $\Delta\Sigma$ modulator, including Jin et al. (2017), Mariano et al. (2012), and Jiang et al. (2008).

Table 5.1 Comparison of the testing time.

Authors	Years	Circuit	Techniques
Jin et al. [16]	2017	SAR ADC	Algorithm Based
Mariano et al. [13]	2012	Time-Interval ADC	Orthogonal Modification
Jiang et al. [7]	2008	DAC & ADC	Polynomial Fitting Algorithm

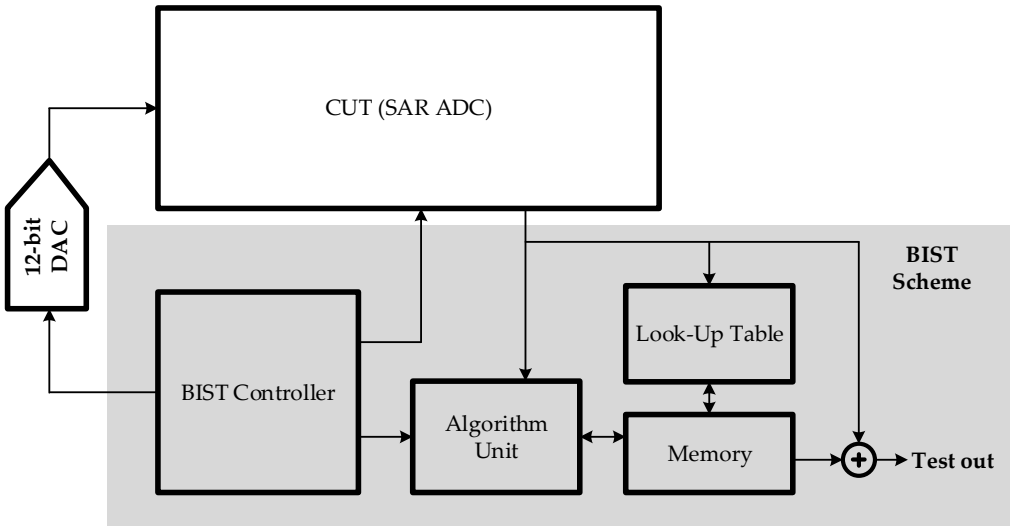

Fig. 5.1 Block diagram of BIST based on stimulus error identification algorithm in ADC (jin et al.)

Jin et al. (2017) [16] introduces an ADC BIST solution based on a segmented stimulus error identification algorithm known as USER-SMILE. This scheme eliminates the requirement to a high-performance external test equipment, and significantly reduces testing time. The core concept is adapting the algorithm for hardware realization. Fig. 5.1 shows the block diagram of BIST based on stimulus error identification algorithm. The 12-bit redundant SAR ADC is used as the CUT. An 12-bit DAC is also used as the test signal generator which insufficient resolution and does not linearity accuracy in order to simply test 12-bit ADC using traditional histogram method. The

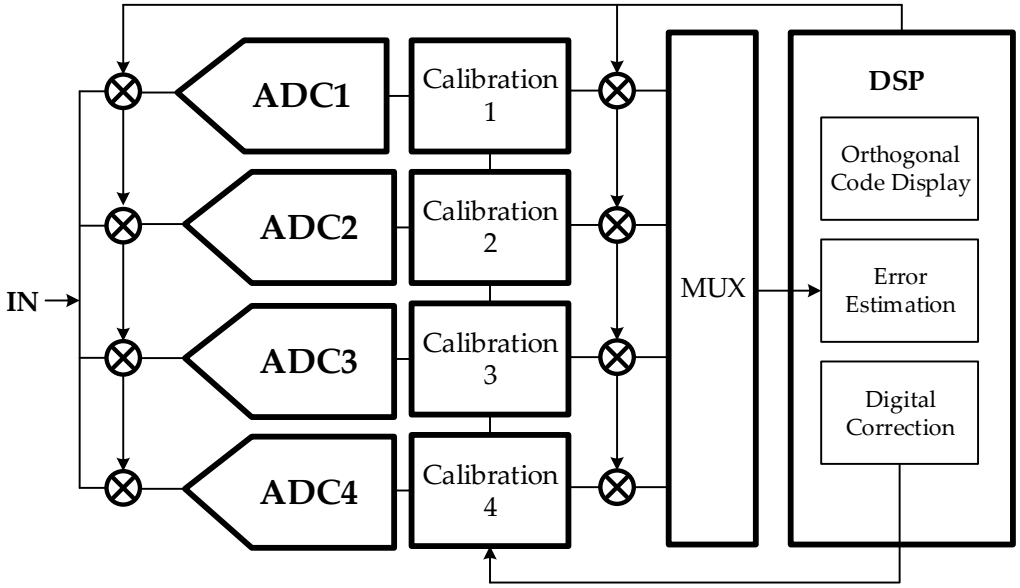

Fig. 5.2 Built-in Self-Calibration (BISC) scheme for Time-Interval ADC (Mariano et al.)

calibration logic is designed through a standalone digital block which provides all required calibration tasks. A small memory is placed to hold intermediate and final test data. The 10dB improvement of SFDR is achieve over without calibration BIST. This approach can extend to calibrate an ADC for superior static and dynamic linearity performance. However, a digital signal processor (e.g., a micro-controller) is required in order to analyze the dynamical performances of the ADC.

Mariano et al. (2012) [13] presents a Built-in Self-Calibration (BISC) scheme for Time-Interval ADC (TIADC). The method can estimate offset, gain and clock skew errors and thus to reduce mismatch effects in the TIADC. Fig. 5.2 depicts the architecture for analog TIADC calibration based on orthogonal modification [15]. The TIADC is used as the CUT, and is implemented with an association of 4 identical ADCs in parallel. The analog inverters (before each ADC) is performed to apply the orthogonal sequences over the input signal previous to ADC. The DSP is employed as the test response analyzer. Significant impact of performances mismatch errors in TIADC, i.e. gain, offset, and timing errors can be reduced. However, this approach is software-

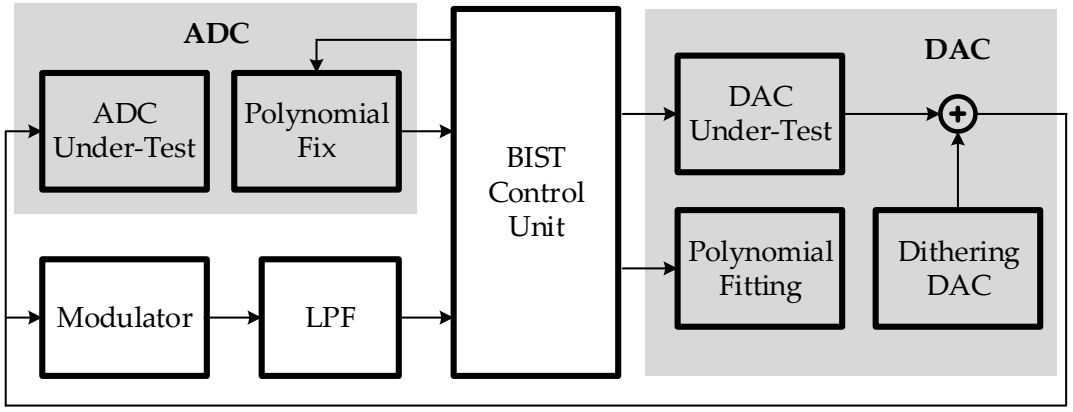

Fig. 5.3 Built-in Self-Calibration (BISC) scheme for Time-Interval ADC (Mariano et al.)

based method which is relatively difficult to practically implement the overall system on a single chip.

Likewise, the BISC of on-chip DAC and ADC is presented by Jiang et al. (2008) [7]. Testing stimulus is provided by a ramps generator circuit. Test responses of DAC-under-test (DUT) are measured by a first-order 1-bit sigma-delta modulator and a low-pass digital filter for noise cancellation as shown in Fig. 5.3. A calibration technique is achieved by a polynomial fit algorithm in order to characterize DAC and to obtain coefficients which can determine whether the DUT passes or fails the test. The integral non-linearity (INL) error is compensated by a dithering DAC with dynamic element matching (DEM) technique. The maximum INL error of ADC and DAC-under-test is reduced from 3 LSB to approximate 0.25 LSB on by compensation signals from dithering DAC, which is verified by simulation results. Although, the linearity of the CUT can be improved, the overall system requires various components such as the low-pass filter, sigma-delta modulator, and dithering DAC, which might be a faulty circuit as well. Additionally, the external DSP is necessary for operating the polynomial fitting algorithm.

It can be clearly seen that the additional digital processor is necessary for BIST and

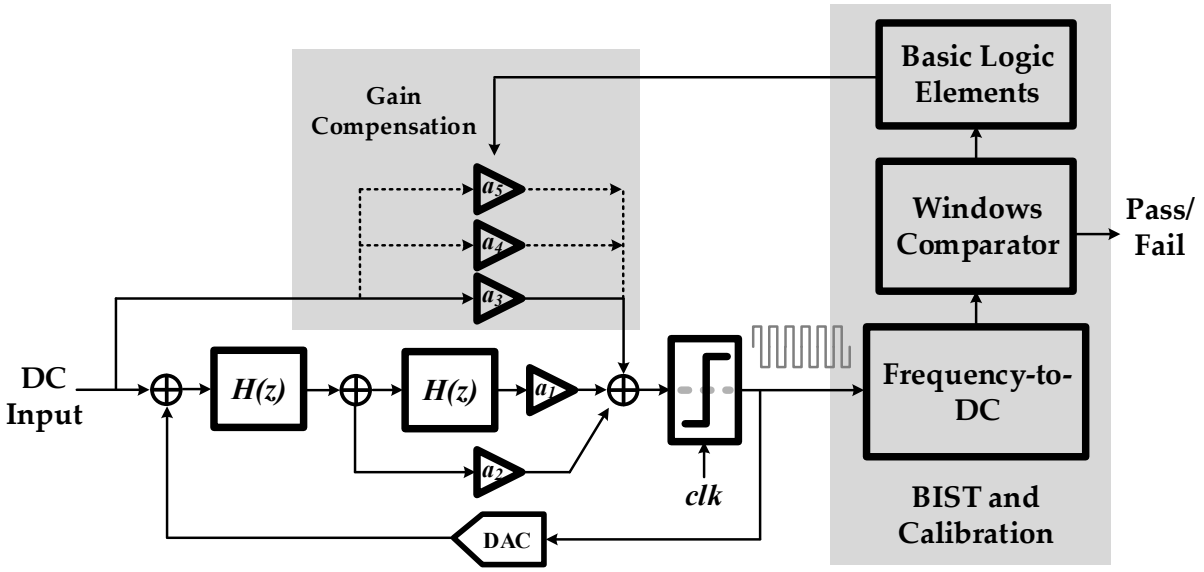

Fig. 5.4 Block diagram of the proposed BIST with self-calibration system.

calibration system, which is relatively difficult to implement entirely on-chip. Another drawback is a requirement of high complexity test response analyzer, which cause the large circuitry of BIST and calibration system. Therefore, this section aims to design a simple BIST and calibration system with high speed and low additional DSP circuitry requirement. Testing and calibration process can be achieved fully on-chip with a practical implementation on 0.18 μm standard CMOS technology.

5.2 Proposed BIST with Self-Calibration System for Analog ΔΣ Modulator

Fig. 5.4 illustrates the block diagram of the proposed BIST with self-calibration system. The system comprises three major building block, i.e. a frequency-to-DC converter, windows comparator, and digital logic elements. Firstly, the DC input is biased to the modulator-under-test (MUT) in order to transform the modulator operation into the oscillation mode, while the testing is enabled. The sinusoidal signals from the MUT

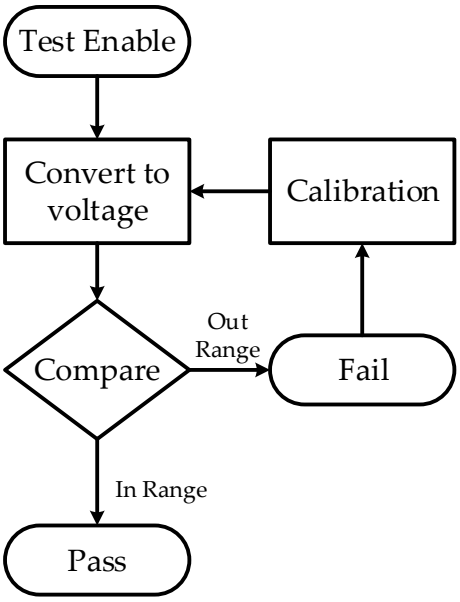

Fig. 5.5 Flowchart of the system operation.

are subsequently converted to the DC voltage by the frequency-to-DC circuitry. Afterward, the converted DC output is characterized by the windows comparator, which provides three properties of the MUT, i.e. faulty, calibration, and fault-free circuit. The calibration process is achieved by the digital logic elements and feedback network. The gain of the MUT is compensated by changing the feed-forward resistor of the integrator. The flowchart of the system operation is also shown in Fig. 5.5

5.3 Overall Circuits Description and Operation

5.3.1 Frequency-to-DC Converter

Fig. 5.6 depicts the schematic of frequency-to-DC converter. The design is based on switching system, which operates on two conditions. Otherwise, in the positive cycle, a half wave current rectifier is formed by transistors M_1 and M_2, which is biased in the weak inversion region through a small DC current source I_B. This rectified current is mirrored and amplified through M_3 and M_4, with the latter operating in the saturation

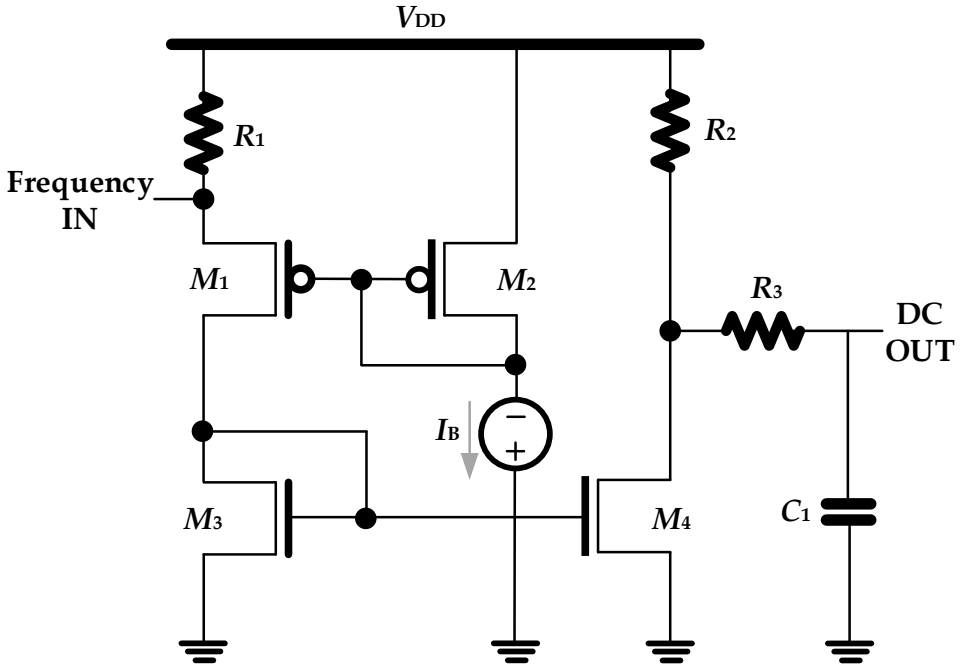

Fig. 5.6 The frequency-to-DC converter.

region. In the negative cycle, the transistor M_1 is operated in cut-off region. A large current swing is only occurred at the transistor M_4 which can preform a half-wave rectification behavior. Afterward, the resultant of current is converted to voltage by resistor R_2. Finally, the DC output is generated through the low-pass filter, forming by R_3 and C_1.

5.3.2 Windows Comparator and Control Calibration Circuit

Fig. 5.7 shows the schematic diagram of the windows comparator and acceptable region of the proposed system. The circuit comprises two ordinary differential amplifiers, NAND, and NOR gates. The fault-free region is determined by V_MAX and V_MIN. In case of the input voltage is deviated from the range of V_MAX and V_MIN, the faulty status is reported, and the calibration process is activated. The control logic B_0 and B_1 defines the feedback gain compensation of the MUT, whether increasing or decreasing.

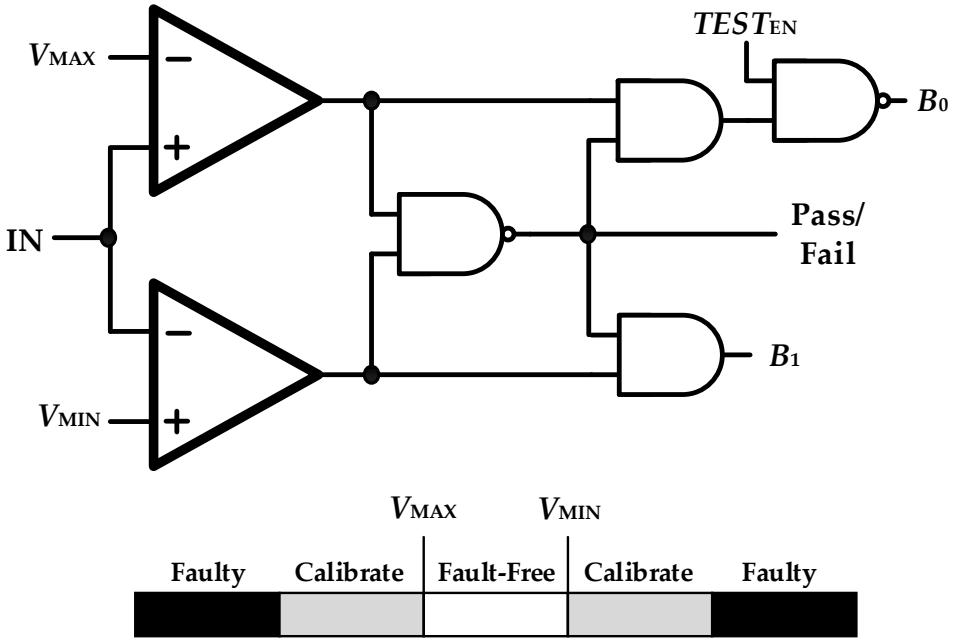

Fig. 5.7 The windows comparator and acceptation regions of the analog circuit.

5.3.3 Continuous-Time Fully Differential 2^{nd}-order $\Delta\Sigma$ Modulator with Gain Compensation

The continuous-time fully differential 2^{nd}-order $\Delta\Sigma$ modulator is illustrated in Fig. 5.8. The feed-forward topology provides high output gain with low distortion and has a higher signal-to-noise ratio (SNR) than an ordinary model. The resistor arrays (gray area) represents the gain compensation technique. The input-output relation of the modulator in the z-domain is given by

$$STF\left(z\right) = \frac{\left(a_1 - a_2 + a_3\right) z^{-2} + \left(a_2 - 2a_3\right) z^{-1}}{\left(a_1 - a_2 + 1\right) z^{-2} + \left(a_2 - 2\right) z^{-1} + 1} \tag{5.1}$$

$$NTF\left(z\right) = \frac{\left(1 - z^{-1}\right)^2}{\left(a_1 - a_2 + 1\right) z^{-2} + \left(a_2 - 2\right) z^{-1} + 1} \tag{5.2}$$

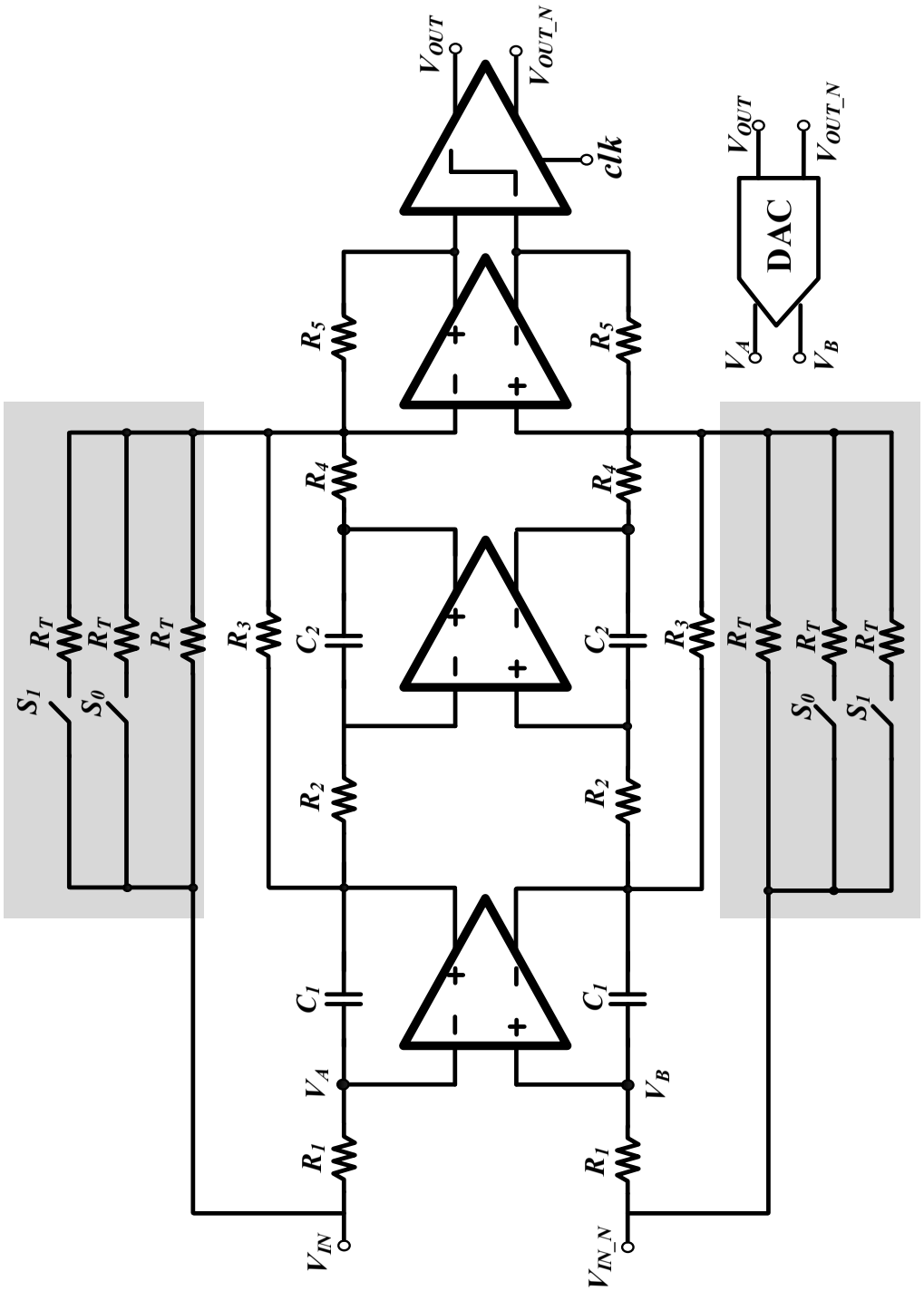

Fig. 5.8 Continuous-time Fully Differential 2^{nd}-order $\Delta\Sigma$ modulator with gain compensation technique

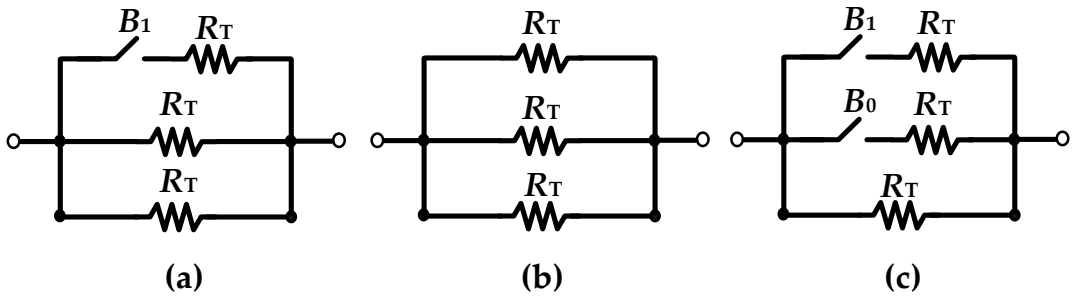

Fig. 5.9 Gain compensation technique (a) normal condition, (b) gain increasing, and (c) gain decreasing.

where the gain parameter a can be defined by the relation of resistor and capacitor value. It can be considered that the system gain a_3 can be adjusted, which provides less effect to the signal transfer function (STF) and does not any impact to the noise transfer function (NTF). Hence, the resister R_T is constructed in terms of stack arrays, and controlled the value by switches S_0 and S_1. Fig. 5.9 shows the gain compensation feature by adjusting the resistor R_T. In the normal condition (Fig. 5.9(a)), the switches S_0 and S_1 are CLOSE and OPEN, respectively. The system gain can be increased by opening the switches S_0 and S_1, and vice versa.

5.4 Simulation Results

The performance of the proposed continuous-time $\Delta\Sigma$ modulator was validated through a HSPICE environment with 2 kHz-input sinusoidal and 1MHz sampling frequency. The resistors R_1 - R_3 and R_4 - R_5 are fixed as 100 KΩ and 50 KΩ, respectively. The capacitor C_1, C_2 are set as 3 pF. Fig. 5.10 exhibits the simulated power spectrum density (PSD) where a 32,768-point FFT with simple rectangular truncation window is employed. The measured maximum SNR was nearly 70 dB and reached 13 bits of the effective number of bits (ENOB). Table 5.2 summarizes the performances of the proposed continuous-time $\Delta\Sigma$ modulator. It is apparent that the resistor arrays for

Table 5.2 Summary performances of the continuous-time ΔΣ modulator

Performances	**Vaules**	**Units**
Power supply	1.8	V
Input frequency	20K	Hz
Oversampling rate	128	-
Max SNR.	70	dB
Power consumption	425.76	µW
Area overhead	0.325	mm^2

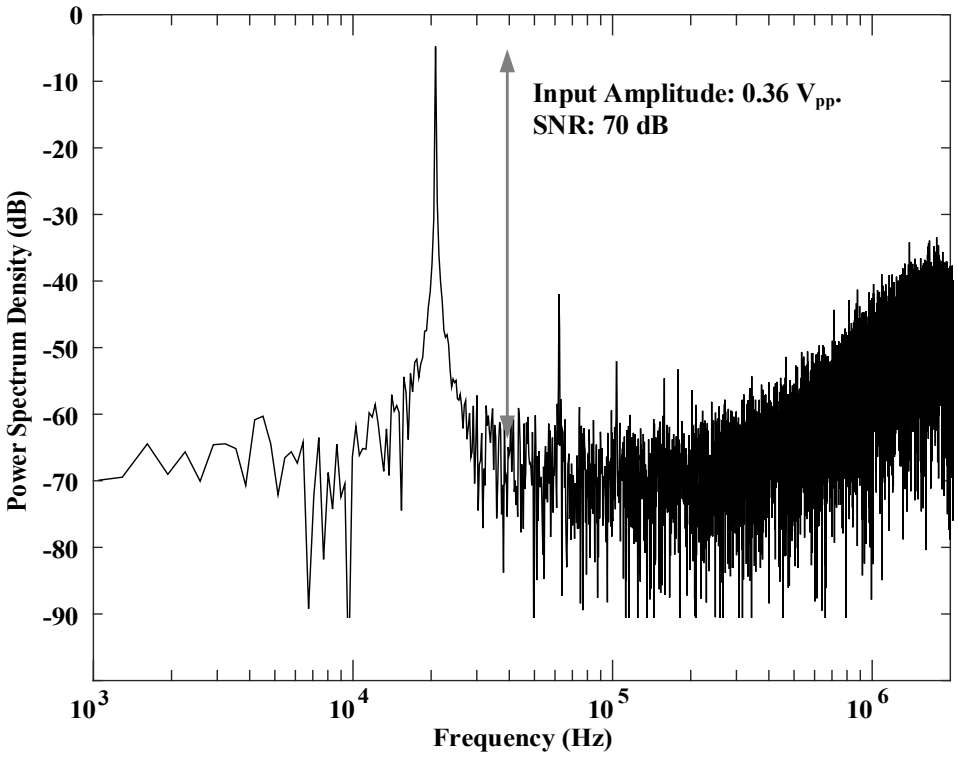

Fig. 5.10 Power spectrum density of the modulator.

gain compensation feature does not degrade the performances of modulator. Likewise, the input-output characteristic of the frequency-to-DC converter is exhibited in Fig. 5.11. The input sweep frequency was measured in range of 500 KHz to 1.8MHz. It can be seen in Fig. 5.11 that the DC output of converter is operated depending on the input frequency. Fig. 5.12 depicts the simulation characteristic of the frequency-

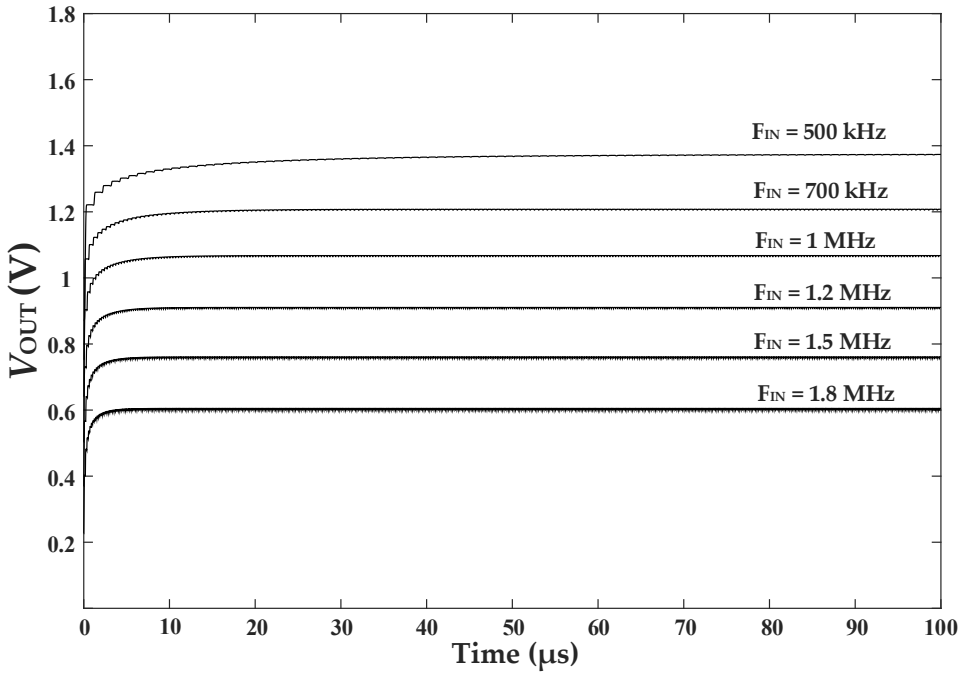

Fig. 5.11 Output characteristic of the frequency-to-DC converter against frequency sweeping.

Table 5.3 Summary of BIST performance

Fault Types	**Details**	**Detectable**
Hard	Short	Yes
Hard	Open	Yes
Hard	GDS	Yes
Soft	-50% at R_1	Yes
Soft	+50% at R_2	Yes
Soft	+50% at C_2	Yes

to-DC converter in fault-free circuit and struck-at fault at transistor gate (GDS). The characteristic indicates that DC output of the frequency-to-DC converter is operated at 0.92V at fault-free condition. On the other hands, the frequency of modulator is decreased, when catastrophic fault is injected, and causes the higher DC output at the frequency-to-DC converter. Table 5.3 summarizes faults detection performance where

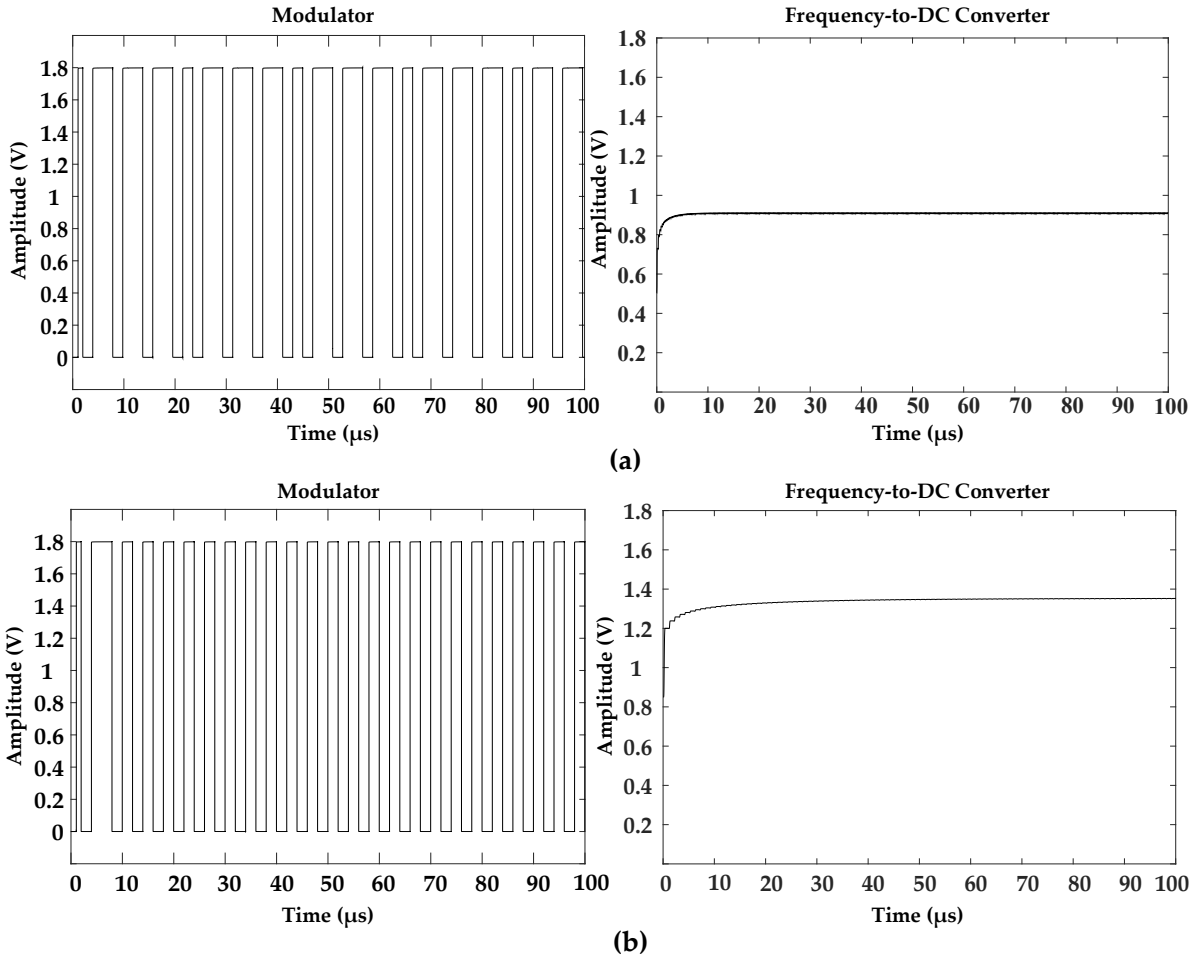

Fig. 5.12 Transient waveform of the modulator and converter where (a) fault-free and (b) catastrophic condition.

V_{MAX} and V_{MIN} of the windows comparator are defined as 1.3 and 0.7, respectively.

The calibration property of the proposed system is also simulated through the SNR measurement of four conditions, i.e. normal mode, +30% in C_1, -30% in C_1 with and without calibration. Fig. 5.13 shows the measured SNR of overall circuits conditions. It can be seen that the SNR of the modulator-under-test can be compensated into the appropriate value, under the deviation of capacitor value (±30%). Fig. 5.14 also exhibits the layout design of proposed system on 0.18 μm CMOS standard technology.

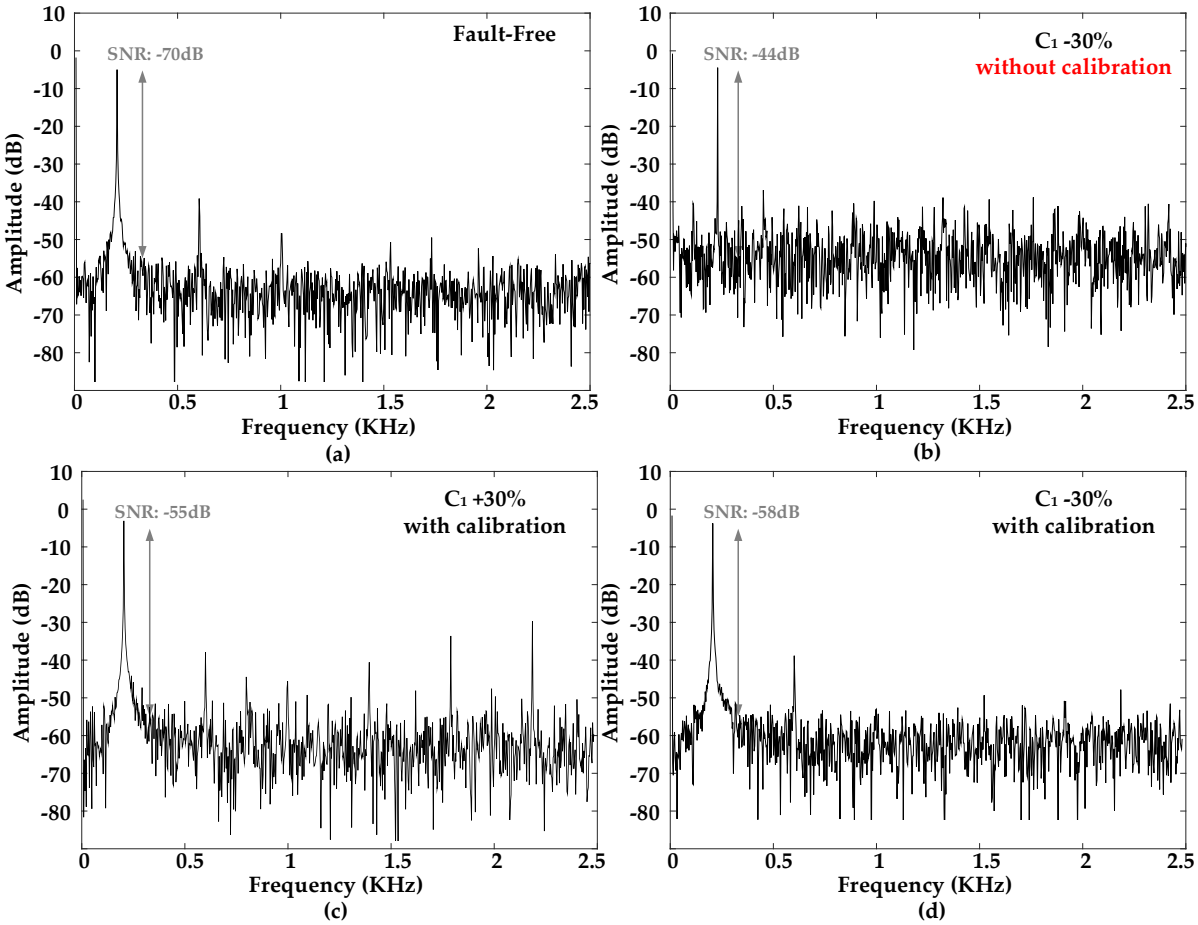

Fig. 5.13 Demonstration of the calibration of SNR in difference circuit conditions (a) fault-free, (b) +30% in C_1 without calibration, (c) +30% in C_1 with calibration, and (d) -30% in C_1 with calibration.

5.5 Conclusion

The BIST method with self-calibration feature for the continuous-time $\Delta\Sigma$ modulator is presented. The proposed system comprises the frequency-to-DC converter, windows comparator, and digital logic elements. The continuous-time fully differential 2^{nd}-order $\Delta\Sigma$ modulator is utilized as the modulator-under-test. The designed modulator with gain compensation is operated correctly in the normal condition. The BIST is achieved, involving catastrophic and parametric faults detectability. Additionally, calibration feature is preformed through feedback network of gain compensation, which

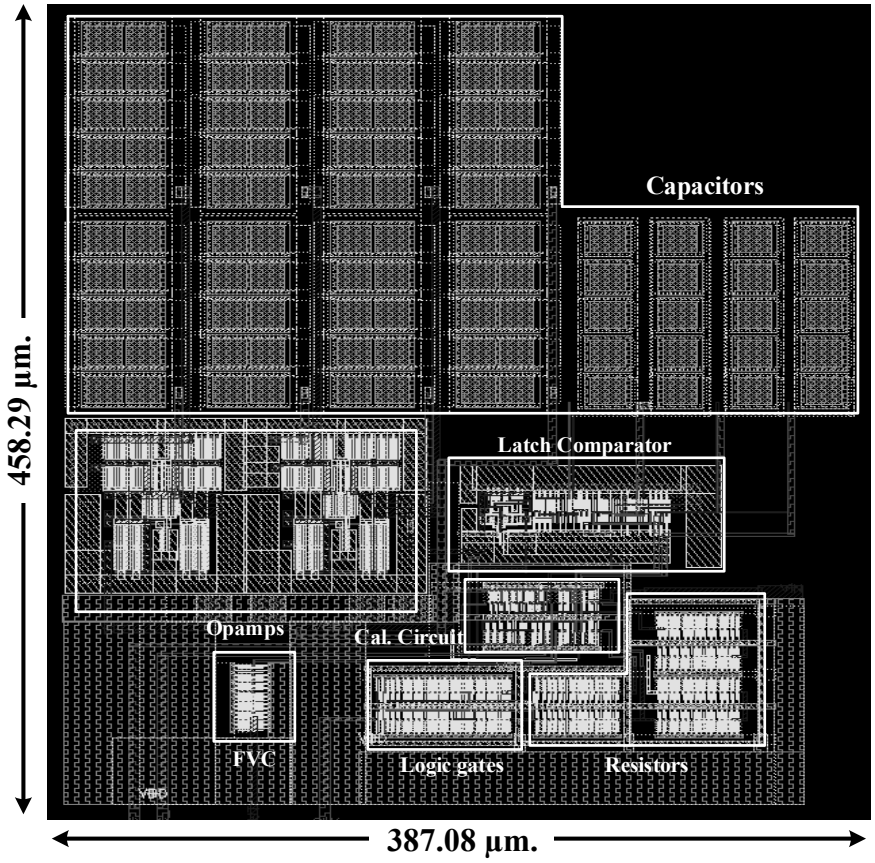

Fig. 5.14 Overall layout diagram of the proposed BIST and calibration technique.

preserve the SNR of the system against the parameter deviation. The overall system is operated and implemented completely on 0.18 μm CMOS standard technology.

5.6 Reference

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Chapter 6

Conclusion

In this dissertation, an improvement design of BIST for an analog and mixed-signals LSI circuit has been presented, involve three major contributions, i.e. test stimulus generation, oscillation-based testing, and a calibration technique. The design strategy is to improve the basic building blocks of BIST, i.e. test stimulus generation, test control, and test response analyzer. Initial introduction of basic background, motivation and objectives of this research have been given in chapter 1.

In chapter 2, the design of a fully-on-chip true-random bit generator has been presented. The chaotic jerk oscillator is employed as an entropy source that provides a robust, a smoothly balanced-to-unbalanced adjustable of double-scroll attractors, and highly phenomenon of chaotic signals. The chaotic dynamics of the oscillator has been examined through the bifurcation diagram, Lyapunov exponents, attractor trajectories and the waveform in time-domain. The widely-used structure of the second-order $\Delta\Sigma$ modulator has been used employed as the circuit-under-test. The modulator was divided into two first-order circuits and executed the chaotic stimulus when the test mode is operated. Faulty circuits have been verified through dissimilarity signals between two divided circuits. Demonstrations of the six different fault types which containing a fault-free, two catastrophic and three parametric faulty circuits have shown the capable to detect all injected faults. This technique eliminates the need of high-precision stimulus generation and simplifies complex faults characterization. The overall system has been fully fabricated on 0.18 μm CMOS standard technology without any digital processing

units. Furthermore, this work has offered a potential alternative for non-intrusiveness BIST with high-speed testing approach in mixed-signal systems.

In chapter 3, a design-for-structural-testability topology for the 2^{nd}-order $\Delta\Sigma$ modulator has been presented. A test operation can be achieved through the structural reconfiguration technique. In other words, circuit structure may be reconfigured and operated as two symmetric circuits structure, thus verifying faulty circuits by the different output waveforms, which can be simply observed through faults signature, indicated by a digital counter circuit. Simulation of the modulator performance also implies the appropriate features with 80 dB for SNR at 128 OSR. Demonstrations of system testability indicated controllability and observability, with simulated test results at 92.86% of total coverage of faults involving catastrophic and parametric defects. This technique eliminates the need for high-precision stimulus generation and simplifies the fault characterization process.

In chapter 4, the BIST based on a phase difference analysis technique for the analog circuits has been presented. The testing technique is based on the detection of phase shifting between a reference clock signal and a modified circuit-under-test (CUT). In the test mode, the designed low-pass filter can be transformed into an oscillator. This technique has provided faults coverage of 96.67%, where all catastrophic fault of the CUT can be detected and the faults tolerance band of all passive components is determined to $\pm$20%. The implemented BIST can eliminate the need for external test equipment by using a compact digital circuit which can be fully designed on-chip.

In chapter 5, the BIST method with self-calibration feature for the continuous-time $\Delta\Sigma$ modulator is presented. The proposed system comprises the frequency-to-DC converter, windows comparator, and digital logic elements. The continuous-time fully differential 2^{nd}-order $\Delta\Sigma$ modulator is utilized as the modulator-under-test. The designed modulator with gain compensation is operated correctly in the normal condition.

The BIST is achieved, involving catastrophic and parametric faults detectability. Simulation of calibration feature indicates the capability of functional circuit preservation under the variation of circuit parameter.

Finally, all of proposed techniques achieve the self-testable property with high faults coverage. Not only catastrophic faults, the parametric variation is also detected through the simulation and experiment measurement. The main functional of circuit-under-test is preserved as their design without any degradation from the BIST system. Overall designed systems are executed and implemented fully on 0.18 μm CMOS standard technology without any external circuitry requirement. These four techniques have offered a potential alternative for an on-chip, non-intrusive and self-testable with high-speed testing approach in mixed-signal systems.

List of Publications

[1] C. Wannaboon, W. San-Um, and M. Tachibana "A 0.18-μm CMOS high-data-rate true random bit generator through $\Delta\Sigma$ modulation of chaotic jerk circuit signals," Chaos: An Interdisciplinary Journal of Nonlinear Science, **Publication process.**

[2] C. Wannaboon, and M. Tachibana "A Design-for-Structural-Testability for Simple Faults Detection in Analog $\Delta\Sigma$ Modulator," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, **Publication process.**

[3] C. Wannaboon, N. Jiteurtragool, W. San-Um and M. Tachibana "Phase Difference Analysis Technique for Parametric Faults BIST in CMOS Analog Circuits," IEICE Electronics Express, vol. 15, 2018

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Authors' Biography

Chatchai Wannaboon received the B.Eng. degrees in Computer Engineering from Thai-Nichi Institute of Technology, Bangkok, Thailand, in 2013 and M.Eng. degrees in Electronic and Photonic System Engineering from Kochi University of Technology, Kochi, Japan, in 2015. He is currently working towards his Ph.D. at the Department of Electronic and Photonic System Engineering, Kochi University of Technology, Japan. His areas of research interests are analog and mixed-signals circuit designs, involving chaotic oscillators and analog-to-digital converter, and on-chip testing design, involving DFT and BIST techniques.