

# Multicore System-on-Chip Based on Low-Power Self-Timed Pipeline

## Project Leader

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## Objective

Our research goal is to establish an architecture for multicore system-on-chip operating at low power consumption. As for future LSI chips, we can integrate over ten billion transistors on a single die. However, in order to improve the performance power ratio of the chip under a specific power budget, it is impossible to operate all transistors on the chip, a problem called utilization wall. The self-timed (clockless) elastic pipeline circuit we have been studying is one promising solution to break through the utilization wall because the self-timed pipeline (STP) itself consumes electric power only at the stage where valid data is processed. We have already succeeded in developing a multicore data-driven processor chip based on the STP and achieved 1/10 lower power than the conventional multicore processors.

## Project Outline

### (1) Multicore SoC power management scheme

In order to overcome the utilization wall, the multicore SoC power management scheme will be studied. In this study, the runtime voltage scaling technique and the fine-grain power gating technique will be utilized to reduce power dissipation as much as possible. The basic power consumption characteristics can be measured by means of our developed LSI chips [2].

### (2) Dedicated accelerator LSI circuit design based on STP

STP is very flexible for implementation of various dedicated functions as reported in [1]. In this study, self-timed low-power circuit for high-speed wireless communication will be designed, e.g., fast Fourier transform (FFT) module, forward error correction (FEC) module.

## References

- [1] Kazuhiro Komatsu, Shuji Sannomiya, Makoto Iwata, Hiroaki Terada, Suguru Kameda, Kazuo Tsubouchi, "Interacting Self-Timed Pipelines and Elementary Coupling Control Modules," IEICE Trans. Fundamentals, Vol.E92-A, No.7, pp.1642-1651, Jul. 2009.
- [2] Hiroaki Nishikawa, Kazuhiro Aoki, Hiroshi Ishii and Makoto Iwata, "Intermediate Achievement of Ultra-Low-Power Data-Driven Networking System: ULP-DDNS", Proceedings of the 2011 International Conference on Parallel and Distributed Processing Techniques and Applications(PDPTA'11), pp.421-427, Las Vegas (USA), July 2011.

## See our admission guidelines:

[https://www.kochi-tech.ac.jp/english/admission/ssp\\_aft19oct/ssp\\_application\\_guideline.html](https://www.kochi-tech.ac.jp/english/admission/ssp_aft19oct/ssp_application_guideline.html)

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