Highly Flexible Integrated System and its Development Platform

Project Leader
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1. Objective

This project is aimed at:

Developing highly flexible integrated systems based on a multi-grained reconfigurable architecture, which can be adopted not only for high-performance computing but also for low-power applications with low hardware cost. We will also develop the CAD tools required for C-based design flows, which can support the implementation of user applications written in ANSI C on our reconfigurable system.

2. Project Outline

To that end, the project will consist of the following phases:

(a) Development of a novel multi-grained reconfigurable architecture

(b) VLSI implementation of the proposed reconfigurable architecture

(c) Development of CAD tools for implementing user applications on our reconfigurable system

3. Expected Performance

In this project, the successful candidate would be expected to:

(a) Working independently with the supervision of the project leader

(b) Assist the senior members with the development of our reconfigurable system

(c) Provide supervision of younger members for developing our reconfigurable system

4. Required Skills and Knowledge

The successful candidate for this project will have the following knowledge and skills:

(a) Computer architecture and FPGA architecture

(b) HDL design and FPGA implementation

(c) C and/or C++ language for computer programming

References

[1] H. Konoura, D. Alnajjar, Y. Mitsuyama, H. Shimada, K. Kobayashi, H. Kanbara, H. Ochi, T. Imagawa, K. Wakabayashi, M. Hashimoto, T. Onoye, and H. Onodera, "Reliability-Configurable Mixed-Grained Reconfigurable Array Supporting C-based Design and Its Irradiation Testing," IEICE Trans. on Fundamentals, vol. E97-A, no. 12, pp. 2518-2529, Dec. 2014.

[2] D. Alnajjar, H. Konoura, Y. Mitsuyama, H. Shimada, K. Kobayashi, H. Kanbara, H. Ochi, T. Imagawa, S. Noda, K. Wakabayashi, M. Hashimoto, T. Onoye, and H. Onodera, "Reliability-Configurable Mixed-Grained Reconfigurable Array Supporting C-To-Array Mapping and Its Radiation Testing," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC 2013)*, pp. 313-316, Nov. 2013.

[3] Y. Mitsuyama, K. Takahashi, R. Imai, M. Hashimoto, T. Onoye, and I. Shirakawa, "Area-Efficient Reconfigurable Architecture for Media Processing," IEICE Trans. on Fundamentals, vol. E91-A, no. 12, pp.3651-3662, Dec. 2008.

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