High-reliability Design and Estimation of Reliability of Advanced Integrated Circuits

Project Leader
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1. Objective

This project is aimed at:
Development of a method of observing the propagation of error inside ICs subjected to environmental noise and a method of designing high-reliability IC to prevent error propagation for complex computation tasks.
Integrated circuits (ICs) consist of numerous basic cells for computation. They are the core components of computers, which serve as the brains of the information society. To support response to the explosively increasing demands for performance of computational tasks in applications such as artificial intelligence (AI), our laboratory is mainly working toward the development of methods for the design of high-efficiency, high-reliability classical ICs. In this project, we mainly address the issue of reliability of ICs subjected to environmental noise in embedded systems. We will develop a method for observing the propagation of error inside existing systems for performing complex computation tasks. Based on our observations, we will establish a propagation model and estimate its error rate during the development of new IC designs or next generation ICs. Finally, we will develop a noise-hardening IC design for use in reliability-critical applications. (Refer to [1-4])
Moreover, for students with a strong interest in quantum computation for the post-CMOS IC era, we will provide further topics related to error correction against environmental noise, toward the realization of practical large-scale quantum computers. (Refer to [5])

2. Project Outline

To that end, the project will consist of the following phases:
(a) Design and conduct simulations/experiments related to error injection for reliability analysis;
(b) Develop an error propagation model and estimate the pre-fabrication error rate of pre-fabrication ICs; and
(c) Design and verify high-reliability ICs, and optimize design for computation efficiency.

3. Expected Performance

In this project, the successful candidate would be expected to:
(a) Work independently in accordance with the agreed research procedures;
(b) Maintain good communication with team members; and
(c) Have strong skills in English writing and presentation for academic purposes.

4. Required Skills and Knowledge

The successful candidate for this project will have the following knowledge and skills:
(a) Self-motivation and strong interest in circuits;
(b) Fluent English (necessary) and Japanese (preferred, related to collaboration in experiments);
(c) Functional level of skill in use of software (C/C++, python etc.) and hardware (e.g., Verilog, VHDL) programming; and
(d) Functional knowledge of VLSI.

References

[1] W. Liao et al., 'Impact of the Angle of Incidence on Negative Muon-Induced SEU Cross Sections of 65-nm Bulk and FDSOI SRAMs', IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1566–1572, 2020.

[2] W. Liao, K. Ito, S.-I. Abe, Y. Mitsuyama, and M. Hashimoto, 'Characterizing Energetic Dependence of Low-Energy Neutron-Induced SEU and MCU and Its Influence on Estimation of Terrestrial SER in 65-nm Bulk SRAM', IEEE Transactions on Nuclear Science, vol. 68, no. 6, pp. 1228–1234, 2021.

[3] T. Tanaka, W. Liao, M. Hashimoto, and Y. Mitsuyama, 'Impact of Neutron-Induced SEU in FPGA CRAM on Image-Based Lane Tracking for Autonomous Driving: From Bit Upset to SEFI and Erroneous Behavior', IEEE Transactions on Nuclear Science, vol. 69, no. 1, pp. 35–42, 2021.

[4] T.-S. Hsu, D.-A. Yang, W. Liao, M. Itoh, M. Hashimoto, and J.-J. Liou, 'Processor SER Estimation with ACE Bit Analysis', in 2021 21th European Conference on Radiation and Its Effects on Components and Systems (RADECS), 2021, pp. 1–5.

[5] W. Liao, Y. Suzuki, T. Tanimoto, Y. Ueno, and Y. Tokunaga, 'WIT-Greedy: Hardware System Design of Weighted ITerative Greedy Decoder for Surface Code', in Proceedings of the 28th Asia and South Pacific Design Automation Conference, 2023, pp. 209–215.

Project leader webpage:

https://www.kochi-tech.ac.jp/profile/en/liao-wang.html

University admission guidelines:

https://www.kochi-tech.ac.jp/english/admission/ssp_aft19oct/ssp_application_guideline.html

Contact

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