Development the Pattern Classification Hardware System based on Artificial Intelligence and Image Processing Technique

Project Leader
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Objective
A system on chip (SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. For developing SOC, pattern classification processing with FPGA can be a real time process and thus have a high-speed advantage. However, intelligent system using pattern classification processing is a special processing method, which requires knowledge of both image processing and development language of FPGA. A system on chip (SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. For developing SOC, pattern classification processing with FPGA can be a real time process and thus have a high-speed advantage. However, intelligent system using pattern classification processing is a special processing method, which requires knowledge of both image pattern classification processing and development language of FPGA.

Project Outline
About this project, it is necessary to learn about intelligent systems and image processing technique, witch is pattern classification technique especially, for ISOC (Intelligent System on Chip). This project will develop the machine system to decide pattern classes using ISOC. For that success, candidates must contribute to design FPGA system using Verilog-HDL. Target is pattern classification of camera images at real-time process. Therefore, candidates need image process technique and Verilog-HDL skill. This project aims at design and implement defect detection software for industrial robot arm products. It also gets signals from a line sensor device for checking surface of the objects. We would like creating a prototype on our lab and needing experiments of image processing of FPGA using camera signal. We need to try some design and test with candidates. In this project I would like to expect to work new design and developing new image process module on FPGA. If candidates provided super vision for image processing using FPGA, we can propose conference and journal as new idea and proposal.

(1) Survey of past research and technical note: pattern classification technique, Verilog-HDL design for FPGA system and image processing using line sensing.
(2) Design the basic image processing system. Experiment is testing with C-language on PC. On this phase, candidates have to create an application of image processing using OpenCV on gcc. And candidates have to redesign image processing to FPGA by Verilog-HDL.
(3) Analysis and review of the experimental and the simulation results about FPGA design. Commencement of design is the pattern classification process. On this phase, candidates have to use simulator system, Model-Sim and Q-sys system from ALTERA.
(4) Design and develop own method about pattern classification processes on the FPGA system. Test and analyze test design on FPGA process simulator. Candidates implement and mount to image processing card, and test using line sensor camera.
(5) Develop the FPGA system on a real FGAP system. Keep testing, data analyzing and growing up proposal process.

References
None.

See my web page:
http://www.ele.kochi-tech.ac.jp/hoshino/

See our admission guidelines:
https://www.kochi-tech.ac.jp/english/admission/ssp/guideline.html

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