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Study on density of states in In-X-Zn-O (X=Sn, Ga) semiconductors and defect passivation methods for highly reliable thin-film transistors

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Study on density of states in In-X-Zn-O (X=Sn, Ga) semiconductors and defect passivation methods for highly reliable thin-film transistors

Jingxin Jiang

Abstract

In this dissertation, the density of states (DOS) in In-X-Zn-O (X=Sn, Ga) semiconductor thin-film transistors (TFTs) were further studied using device simulation. In addition, I proposed a novel fluorine (F) reduction and/or passivation of DOS method to improve performance and stabilities for oxide TFTs. Highly stable fluorine-passivated In-Ga-Zn-O (IGZO) TFTs were developed through long time annealing. Advanced optimization of fabrication parameters of F concentration in fluorine silicon nitride (SiN_X:F) passivation were further discussed. We successfully achieved high performance fluorine-passivated IGZO TFTs by reducing the annealing time through increasing the F concentration in fluorinated silicon nitride passivation layer. In addition, I developed novel bottom-gate self-aligned oxide TFTs with thermally stable S/D regions formed by direct deposition of SiN_X:F on top of the IGZO film. The main works and results of this thesis will be exhibited by 7 chapters.

Chapter 1 Introduction

The background to current researches on TFTs was investigated. Due to the limitation of the mobility for hydrogenated amorphous silicon (a-Si:H), amorphous oxide semiconductor (AOS) is expected to be alternative candidate material for TFTs. However, some issues remain before commercial application can be realized. In order to solve these remaining issues, the objectives of thesis were proposed and the outline of thesis was built.

Chapter 2 Fabrication techniques and characterization techniques for TFTs

The working principles, apparatus structures and parameters of the fabrication techniques (magnetron sputtering, plasma enhanced chemical vapor deposition, inductively-coupled chemical vapor deposition) and characterization techniques (X-ray

photoelectron spectroscopy, secondary ion mass spectrometry, TFTs evaluation system, and device simulation) were systematically described.

Chapter 3 Study on density of states of a-In-X-Zn-O (X=Ga, Sn) TFTs using device simulation

The DOS models of In-X-Zn-O (X=Sn, Ga) TFTs were set up using device simulation. The influence of DOS on electrical properties of bottom-gate amorphous InSnZnO (a-ITZO) and IGZO TFTs were studied. The difference between the influence of front- and back-channel interface traps on subthreshold swing (S) and turn on voltage (V_{on}) of a-ITZO TFTs with different channel thicknesses was further analyzed using device simulation. Deterioration of S and positive shift of V_{on} were observed when front-channel (N_{af}) or back-channel (N_{abk}) interface traps increased. Influence of N_{af} was stronger than N_{abk}. However, the influence of N_{af} on S was not dependent on ITZO thickness (T_{ITZO}); furthermore, variations of N_{af} on S and V_{on} were hardly dependent on T_{ITZO}. On the other hand, variations of S and V_{on} became larger for thinner T_{ITZO} TFT when N_{abk} varied; these phenomena can be explained by considering the screening length. It was confirmed that not only N_{af} but also N_{abk} are important factors of S and V_{on} to fabricate high performance thinner oxide TFT.

Chapter 4 Highly stable fluorine-passivated IGZO TFTs through long time annealing

The electrical properties and stabilities of IGZO TFTs with SiO_X and SiN_X:F passivation were investigated. Highly stable fluorine-passivated IGZO TFT was developed through long time annealing. The defects in the IGZO TFT were passivated by fluorine, which was introduced into a SiO_X etching stopper during the deposition of fluorinated silicon nitride for passivation and diffused during post-fabrication annealing. Using secondary ion mass spectrometry analysis, the reliabilities of the IGZO TFT under positive bias and temperature stress (PBTS), negative bias illumination stress (NBIS) were observed to be markedly improved when fluorine diffusion was detected in the IGZO channel. Improvements in performance and stabilities of IGZO TFTs were

achieved by fluorine-passivated IGZO TFT. The fluorine-passivated IGZO TFT has improved operation temperature, passivates deep defects and is thus advantageous for achieving high-performance and high-reliability oxide TFTs for next-generation displays.

Chapter 5 Highly stable F+ passivated IGZO TFTs

Based on chapter 4, the fabrication parameters of F concentration in SiN_X:F passivation were further optimized. We successfully fabricated high performance fluorine-passivated IGZO TFTs by reducing the required annealing time through increasing the F concentration in SiN_X:F passivation layer. SIMS results revealed that 1h annealing is sufficient for F diffusion from the SiO_X-ES layer to the IGZO channel, if larger F existed in the SiO_X-ES layer. The fluorine-passivated IGZO TFT has highly stable stabilities under PBTS, NBIS, Positive constant current stability (CCS) and good uniformity, which is advantageous for developing high-performance and high-reliability oxide TFTs for use in future electronic devices.

Chapter 6 Self-aligned bottom-gate IGZO TFT with source/drain regions formed by direct deposition of fluorinated silicon nitride

We developed a bottom-gate and self-aligned IGZO TFT with source and drain (S/D) regions that were formed by a direct deposition of SiN_X:F on top of the IGZO film (IGZO/SiN_X:F). The resistivity of IGZO/SiN_X:F stack for the S/D regions of the TFT ($\rho_{S/D}$) was highly stable after annealing, and it obtained 4.1×10^{-3} Ωcm after N_2 annealing at 350 °C. As a result of thermally stable $\rho_{S/D}$, the TFT properties with the IGZO/SiN_X:F S/D regions improved drastically compared with those of IGZO/SiO_X S/D regions. The field effect mobility of 10.6 $cm^2V^{-1}s^{-1}$ and an ON/OFF current ratio of over 10^8 were obtained after 300 °C annealing. The proposed method is crucial for making thermally stable S/D regions for self-aligned oxide TFTs.

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Chapter 1
Introduction

1.1 The overview of thin-film transistors

Since Alessandro Volta first introduced the term “semiconducting” in 1782 [1], semiconductors have changed the world to an extent beyond anything that could have been imagined. The history of semiconductors really dates to 1833, when Michael Faraday was able to scientifically observe the semiconductor effect in an experiment that showed how the electrical conductivity of silver sulfide increased with increasing temperature. Since the first semiconductor effect was recorded [2], the semiconductor industry has spread to every corner in the world and semiconductors have become part of our daily life.

Based on the understanding of the Scottky diode, a metal-semiconductor contact in 1939 [3], Shockley developed an electronic switching device that effectively represents the metal-semiconductor field-effect transistor (FET) invention. Thin-film transistors (TFTs) are a special kind of FET made by deposition of thin films of semiconductor layer as well as the dielectric layer and metallic contacts on a substrate. The history of the TFT really began with the work of P.K. Weimer at RCA Laboratories in 1962 [4]. Weimer invented a staggered structure TFT, with the source and drain contacts on the opposite side of the film from the gate. The channel layer of TFTs can be made using a wide variety of semiconductor materials such as silicon, polycrystalline silicon (poly-Si), compound semiconductors and organic semiconductors. High mobility, uniform, and stable TFT technology for large-area electronics has attracted much attention for application in next generation flat-panel displays (FPDs) such as super-high-definition (SHD) TVs, organic light emitting diode (OLED) displays, and 3D displays.

1.1.1 a-Si:H TFTs

Since their first demonstration in 1976 by Madan, LeComber and Spear [5], amorphous silicon TFTs (a-Si TFTs) have been used in the active-matrix addressing circuits in flat panel displays, optical scanners and x-ray image sensors [6,7] However, the main feature of amorphous materials is the disorder of atomic structure. So there is a

very high defect density in amorphous silicon, which limits its application in making semiconductor devices. Hydrogenated amorphous silicon (a-Si:H) has a sufficiently low number of defects and has been extensively investigated for use in flexible electronics, and has a demonstrable ability to be fabricated into flexible solar cells and TFTs [8–11]. Since a-Si:H TFTs were described by Lecomber et al. in 1979 [12], a-Si:H TFTs have been in widespread use by the active-matrix liquid crystal display (AMLCD) industry. However, a critical technical issue associated with employing a-Si:H TFT backplanes on clear plastic substrates for organic light emitting diodes (AMOLEDs) displays is the stability of a-Si:H TFTs. The threshold voltage of a-Si:H TFTs increases with time due to charge trapping in the gate insulator and defect creation in the a-Si:H [13]. This problem becomes serious when the TFTs are made at the low process temperatures compatible with existing clear plastic substrates (<< 300 °C). Moreover, device performance is limited by the low field effect mobility of the channel materials. As shown in Fig. 1.1, for a-Si:H, sp^3 orbitals which comprise the conduction band have strong directivity; therefore, the bond angle fluctuation in amorphous phase leads to high density of tail states. Carrier transport in a-Si:H is controlled by hopping between localized tail states and conduction band. Therefore, the mobility of a-Si:H is limited to below 1 $cm^2V^{-1}s^{-1}$ [14].

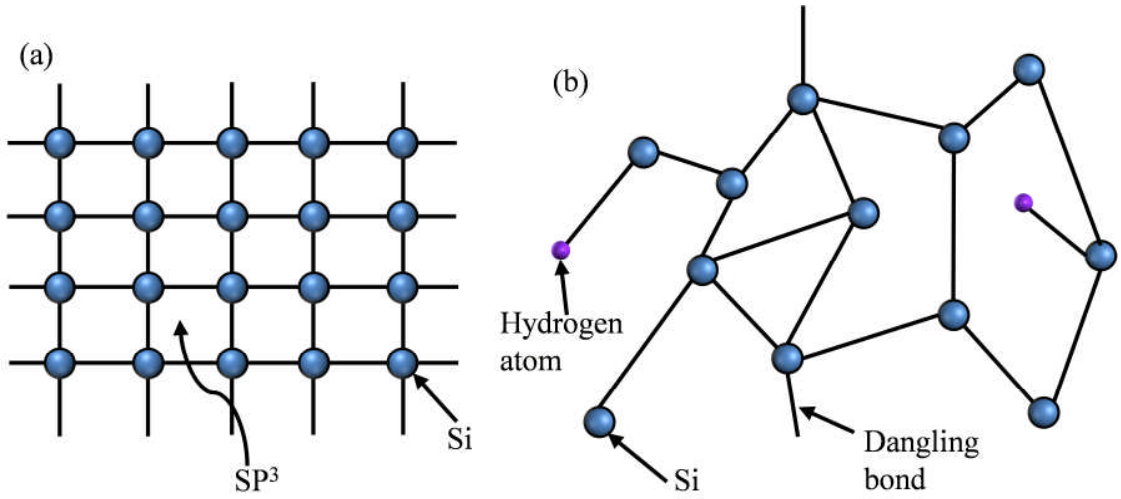

Fig. 1.1 Schematic orbital drawings for the carrier transport paths of covalent semiconductors in (a) crystalline and (b) amorphous. (adapted from [13]).

For AMLCDs, low mobility of ~0.5 $cm^2V^{-1}s^{-1}$ for a-Si:H TFTs is sufficient for driving the present high-definition (HD) AMLCDs of less than 90 inches diagonal size, and the instability can be compensated by LCD driver circuits. However, further high-definition LCDs such as ultra-high-definition (4K) LCDs (e.g. 55 inches) with high frame rates driving with 120 Hz [15,16] require higher mobility for drive; the required mobility will be proportional to the resolution of the display and driving frame rate. Especially, three-dimensional (3D) displays must project two or more picture frames alternately for the left and right eyes. To improve the picture quality, higher frame rates of about 480 Hz are required. The mobility required to drive high-definition LCDs can be expressed as the following equation (1.1).

$$\mu >> \frac{(C_{LC}+C_S)}{\frac{W}{L}C_i(V_G-V_t)} \times f_R \times n \qquad (1.1)$$

Where C_{LC} is liquid crystal capacitance, C_S is storage capacitance, n is number of scan line and f_R is driving frame rate. Required mobility is proportionate to no. of scan line and driving frame rate. Fig. 1.2 shows the required mobility of TFT as functions of the number of pixels in the display. Since mobility of amorphous silicon TFT is below 1 $cm^2V^{-1}s^{-1}$, 4K×2K with 60Hz driving may be the maximum resolution. To achieve super high definition, mobility must be over 10 $cm^2V^{-1}s^{-1}$, which is an impossible value to achieve with current amorphous silicon technology.

1.1.2 Amorphous oxide TFTs

TFT large area applications include switching and driving devices for active matrix flat panel displays (AMFPDs) based on AMLCDs and AMOLEDs, medical imagers, pressure sensors, low-power communication and energy harvesting [17-22]. With the rapid development of the requirements of TFTs in large area electronics, different TFT technologies, like a-Si:H, poly-Si, organic semiconductors and metal oxides have received considerable attention from researchers.

The comparisons between different TFT technologies are summarized in Table 1-1. We find that poly-Si TFT has better electrical properties than a-Si:H, such as high carrier mobility (> 100 $cm^2V^{-1}s^{-1}$) , excellent bias and light stability [23]. Moreover, it is also

possible to fabricate poly-Si devices on cheap glass substrates by excimer laser annealing (ELA) at a comparatively low temperature of about 250 °C, enabling its application even in flexible electronics. However, the main drawback of poly-Si TFTs is the uniformity and scalability due to grain boundaries. So poly-Si can only be widely applied in lightweight, portable, low power and high resolution FPDs, such as smart phones, personal digital assistants, and laptop personal computers. On the other hand, as explained in the last section, a-Si:H has many problems such as low mobility (<1 $cm^2V^{-1}s^{-1}$), instability under illumination (the Staebler-Wronski effect [24–26]) and electrical bias stress. It is assumed that a-Si:H TFTs will be difficult to apply in the future mass production of OLED displays. Although organic TFT technology is compatible with large area processes and can be fabricated at low temperature, the low carrier mobility and electronic and illumination stability of TFTs remain a critical issue.

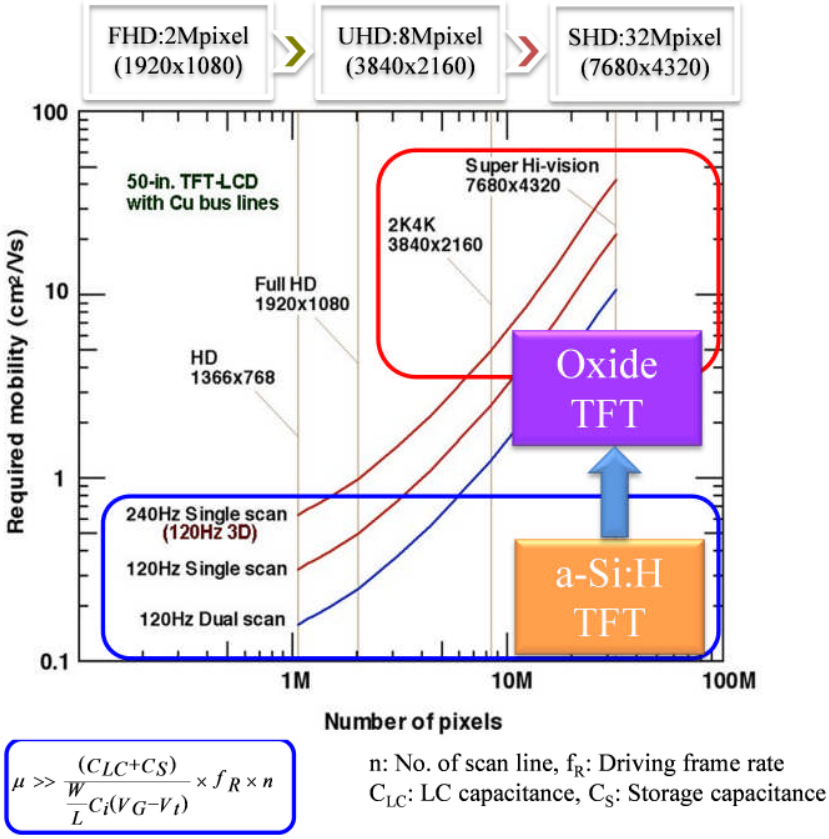

Fig. 1.2 Requirement of mobility for higher-definition FPDs. (Ref. Matsueda, ITC 2010, p.314)

Table 1.1 Comparison different TFT technologies.

Items	Poly-Si TFT	a-Si:H TFT	Organic TFT	a-metal oxide TFT
Mobility	~100	<1	1-10	>10
Uniformity	Poor	Good	Poor	Good
Scalability	4 G	>10 G	8G	8 G
Reliability bias stress	Very good	Poor	Poor	Good
Reliability light stress	Very good	Poor	Poor	Poor
TFT mask	5-9	4-5	4-5	4-5
Cost/yield	High/low	Low/high	Low/High	Low/high
Processing temp.	250-550 ℃	~250 ℃	<200 ℃	RT-400 ℃
Deposition method	PECVD+ELA	PECVD	Printed, solution	Sputtering
band gap	~1.5 eV	~1.7 eV	2-3 eV	~3 eV

Amorphous metal oxide semiconductors (AOS) are expected to be alternative material for TFTs. AOS TFTs have an excellent uniformity owing to their amorphous structure without grain boundaries, and their stabilities under electrical stresses are much better than those of either a-Si:H or organic TFTs. What is more, metal oxide semiconductor has ns orbital, as shown in Fig. 1.3. Isotropic shape and direct overlap among the neighboring metal ns orbitals, ensuring high mobility is even at amorphous structure [14]. Whereas the mobility of a-Si is difficult to improve, oxide TFTs have mobility of over 10 $cm^2V^{-1}s^{-1}$, and are compatible with OLEDs, large LCDs and high-frame-rate 3D displays; so transparent amorphous oxide TFTs will be a strong candidate for future super high definition FPDs. In addition, AOS TFTs can be fabricated at low temperatures or even at room temperature with annealing temperature below 400 °C. Thus, AOS TFTs are compatible with the present FPD industry using large cheap glass substrates.

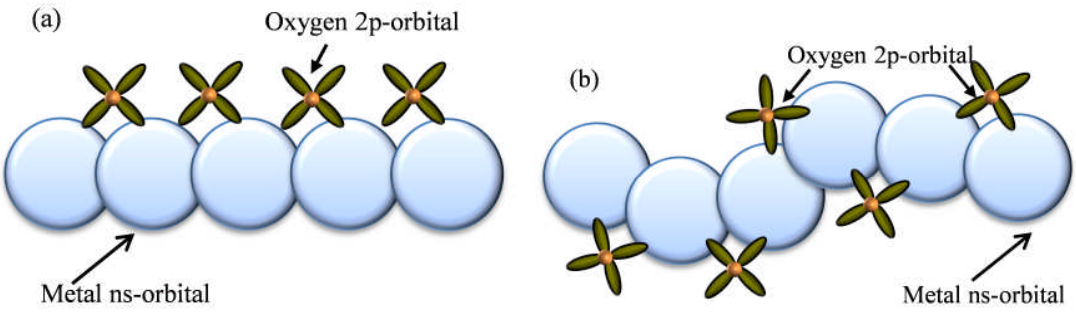

Fig. 1.3 Schematic orbital drawings for the carrier transport paths of post transition metal oxide semiconductors in (a) crystalline and (b) amorphous. (adapted from [13]).

1.1.3 Current remain issues of AOS TFTs

In late 2004, Nomura et al. reported that a representative AOS, amorphous In-Ga-Zn-O (a-IGZO), applied on transparent and flexible TFTs [14]. Since then, AOS TFTs have attracted considerable attention for use in next generation large-area FPDs [27,28]. However, further improvement of their electrical properties is required for the realization of next generation of FPDs. Since the electrical properties of oxide TFTs are highly dependent on the density of localized states (DOS), there have been many studies of the effects of the DOS in oxide semiconductor on the electrical properties of TFTs [29-33]. In order to clarify the physics and electrical properties of oxide TFTs, it is very essential to set up the physical models using a two-dimension (2D) device simulation (ATLAS). Moreover, AOS TFTs still have issues that need to be solved before practical application can be realized. Bias stress instability [34-36], especially at high operating temperature [37,38], is of crucial importance for their practical application; further improvement of bias stability at high operation temperature is also required. Furthermore, it is recognized that the negative bias illumination stress (NBIS) is a crucial issue of instability under light illumination especially for their unique transparent circuit and AMLCD applications [39,24-26], since TFTs are frequently negatively biased and exposed to backlight or ambient light during operation. K. Nomura et al. reported that a-IGZO contained high-density deep subgap defects with energy level closed to the valence band maximum (near VBM state) at the IGZO back-channel surface within ~2 nm [26]. The TFT degradation induced by NBIS stress is strongly affected by the density of deep defects [40]. Therefore, it is very important to reduce the defects in order to improve the stability of oxide TFT. Reduction and/or passivation of DOS are an effective method to improve performance and stabilities for oxide TFTs.

In additional, a bottom-gate with an etch-stopper structure has been widely employed for oxide TFTs. However, one serious drawback of this structure is large parasitic capacitance of gate-to-drain (C_{GD}) and gate-to-source (C_{GS}), owing to the overlap between gate and source/drain (S/D) electrodes. It is known that the parasitic capacitance reduces the operation speed of the TFT circuits, and induces signal delay in the TFT backplane [41]. A self-aligned structure is essential for oxide TFTs to achieve system-on-panel and high-resolution LCD and OLED displays. It was reported that the performance

of self-aligned IGZO TFTs with S/D regions doped by H_2 or Ar plasma treatment is easily degraded after thermal annealing around 200-250 °C [42-47]. Therefore, it is necessary to develop a novel method for making thermally stable self-aligned oxide TFT with highly conductive S/D region. Further research on the DOS of oxide TFTs, novel passivation methods and novel thermally stable self-align structure for achieving high-performance and highly reliable TFTs is therefore essential.

1.2 Objective and structure of the thesis

In my thesis, the influence of the DOS in In-X-Zn-O (X=Sn, Ga) semiconductor on electrical properties of TFTs was further analyzed using device simulation. Based on this study, a method of reducing the DOS in a-IGZO is investigated. We successfully developed a novel F passivation method of oxygen deficiencies using fluorinated silicon nitride (SiN_X:F) as a fluorine source. It was found that the stabilities of the IGZO TFT with SiN_X:F passivation were markedly improved when the diffusion of F into the IGZO channel from a SiO_X etching stopper (SiO_X-ES) was confirmed after post-fabrication annealing. Finally, high performance fluorine-passivated IGZO TFTs were successfully achieved by reducing the annealing time through increasing the F concentration in SiN_X:F passivation layer. The fluorine-passivated IGZO TFT has enhanced operating temperature, passivates the deep defects near VBM and is advantageous for achieving high-performance and high-reliability oxide TFTs for next-generation displays.

As mentioned above, AOS TFTs have accelerated the industrial development of next generation FPDs such as SHD TVs, OLED displays, and 3D displays. For an OLED display, large C_{GD} of selecting TFT in a pixel strongly influences the uniformity of luminescence of pixels. In order to achieve system-on-panel and high-resolution LCD and OLED displays, the main objective are to concentrate on developing a self-aligned structure oxide TFT. To this end, I developed a bottom-gate and self-aligned IGZO TFT with S/D regions that were formed by a direct deposition of SiN_X:F on top of the IGZO film (IGZO/SiN_X:F).

My dissertation consists of seven parts, the organization of which is shown in Fig. 1.4.

The first chapter introduces the background and motivation for my research.

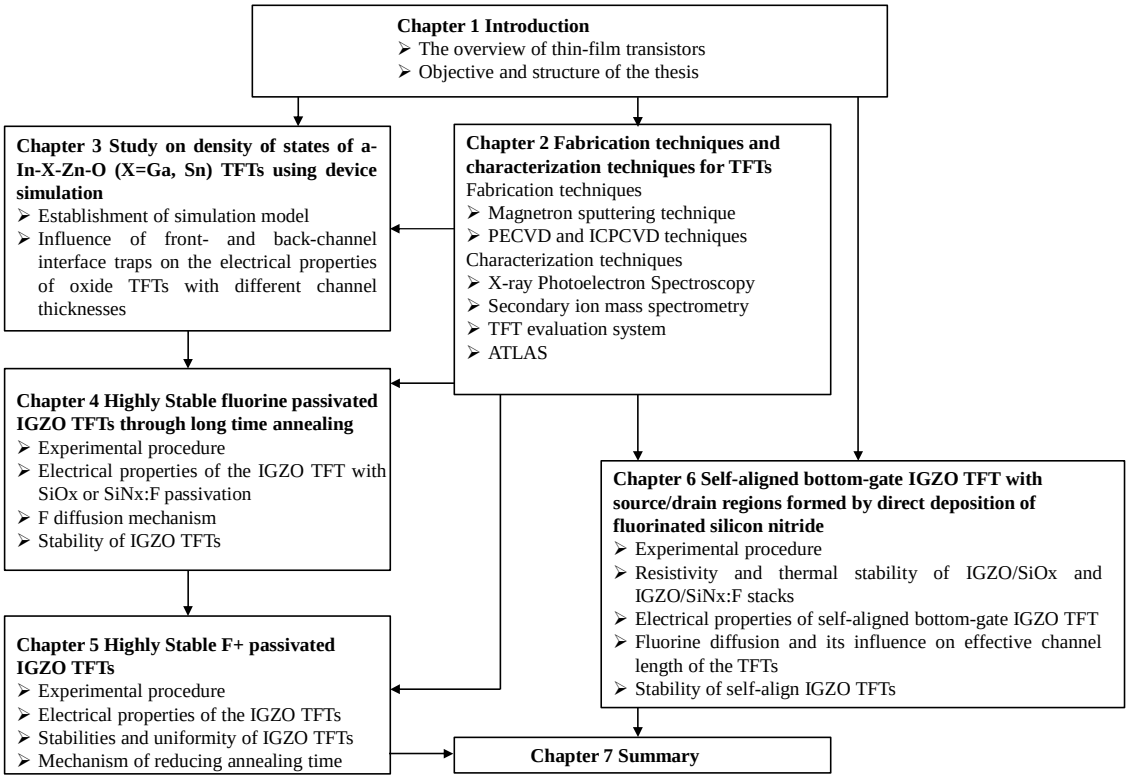

Fig. 1.4 The organization chart of this thesis.

Chapter 2 briefly introduces the working principles, apparatus structures and parameters of fabrication equipment and characterization devices. In this study, TFTs with different deposition parameters were prepared using fabrication techniques. Following the preparation of the samples, different characterization techniques were used to evaluate electrical properties, chemical properties, element profile and structure.

In chapter 3, the DOS model of In-X-Zn-O (X=Sn, Ga) TFTs is set up using device simulation. The influence of DOS on electrical properties of bottom-gate amorphous InSnZnO (a-ITZO) and IGZO TFTs with different channel thicknesses are studied. The influence of localized interface traps on the subthreshold swing (S) and turn on voltage (V_{on}) with different thicknesses is discussed in detail, by means of device simulation. It is confirmed that not only front-channel interface traps but also back-channel interface traps are important factors of S and V_{on} for thinner channel TFTs in order to achieve high performance oxide TFTs.

In chapter 4, the electrical properties and stabilities of IGZO TFTs with SiO_X and

SiN_X:F passivation are investigated. Improvements in performance and stabilities of IGZO TFTs were achieved by SiN_X:F passivation as compared with SiO_X passivation after long time annealing. Highly stable fluorine-passivated IGZO TFT was developed through long time annealing. It was found that F can effectively passivate oxygen vacancy, weakly bonded oxygen in IGZO bulk and/or at front interface, resulting in improved performance and stabilities of IGZO TFTs.

Advanced optimization fabrication parameters of F concentration in SiN_X:F passivation were further discussed in chapter 5. The electrical properties and stabilities of highly Stable F+ passivated IGZO TFTs were investigated. Finally, we successfully achieved high performance fluorine-passivated IGZO TFTs by reducing the annealing time through increasing the F concentration in SiN_X:F passivation layer.

In chapter 6, we developed a bottom-gate and self-aligned IGZO TFT with S/D regions that were formed by a direct deposition of SiN_X:F on top of the IGZO film (IGZO/SiN_X:F). The resistivity of IGZO/SiN_X:F stack for the S/D regions of the TFT was highly stable after annealing, and it obtained 4.1×10^{-3} Ωcm after N_2 annealing at 350 °C (resistivity of as-fabricated IGZO/SiN_X:F stack was 3.3×10^{-3} Ωcm.). So, the TFT properties with the IGZO/SiN_X:F in the S/D regions improved drastically compared with those of IGZO/SiO_X in the S/D regions. The stabilities of BGSA IGZO TFT were also investigated at different bias stress with or without illumination.

Chapter 7 summarizes this thesis work.

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Chapter 2

Fabrication techniques and characterization techniques for TFTs

In the term of fabrication techniques, the basic deposition theory including magnetron sputtering, plasma-enhanced chemical vapor deposition (PECVD) and inductively coupled plasma chemical vapor deposition (ICP-CVD) technique is described in detail.

In order to evaluate the structural and electrical properties of stacked films and TFTs, four kinds of characterization methods were carried out. The chemical and structural evolution of a-IGZO with SiO_X and SiN_X:F films were analyzed by X-ray photoelectron spectroscopy (XPS). The depth profile in ES/IGZO/Si stacked layers for SiO_X or SiN_X:F passivation was analyzed by secondary ion mass spectrometry (SIMS). The electrical properties and stabilities of TFTs were measured in dark chamber with/without a heater, or a light using an Agilent 4156C precision semiconductor parameter analyzer. The simulation model of oxide TFTs was set up by device simulation. The basic theory of the characterization devices was systematically descripted in this chapter.

2.1 Fabrication techniques

2.1.1 Magnetron sputtering technique

Sputter deposition is a physical vapor deposition (PVD) method for depositing thin films, and is one of the most popular growth techniques due to its low cost, simplicity, large area, and low deposition temperature [1]. The term sputtering means to eject material from a target and then deposit it on the substrate. Magnetron sputtering can be classified into direct current (DC) and radio frequency (RF) modes. In this thesis, an active layer was fabricated using DC magnetron sputtering, as shown in Fig. 2.1.

In terms of magnetron sputtering system, magnets are used to increase the percentage of electrons that are active in ionization of events and thereby increase the probability of electrons striking the argon atoms, increase the length of the electron path, and hence increase the ionization efficiency significantly.

The kinetic energy loss of ejected species from the target to substrate is affected by the deposition parameters. The kinetic energy of species is inversely proportional to the deposition pressure. Here, the mean free path can help us to understand the phenomenon [2]. The mean free path (λ_{free}) of molecules is the average distance the particle travels

between collisions with other moving particles, which can be expressed as the following equations.

$$\lambda_{free} = 1/(\sqrt{2}\,\pi\sigma^2 n) \tag{2.1}$$

where $\pi\sigma^2$ is a collision cross section. n is molecular density.

$$\lambda_{free} = \lambda_0(\frac{T}{273})\frac{1}{p} \tag{2.2}$$

λ_0 is a constant at 1 Torr and 0 °C. Taking argon gas as an example, the λ_0 is 0.48. When the thin films are deposited under high deposition pressure, ejected species will suffer many more collisions to shrink the mean free path, resulting in more kinetic energy losses.

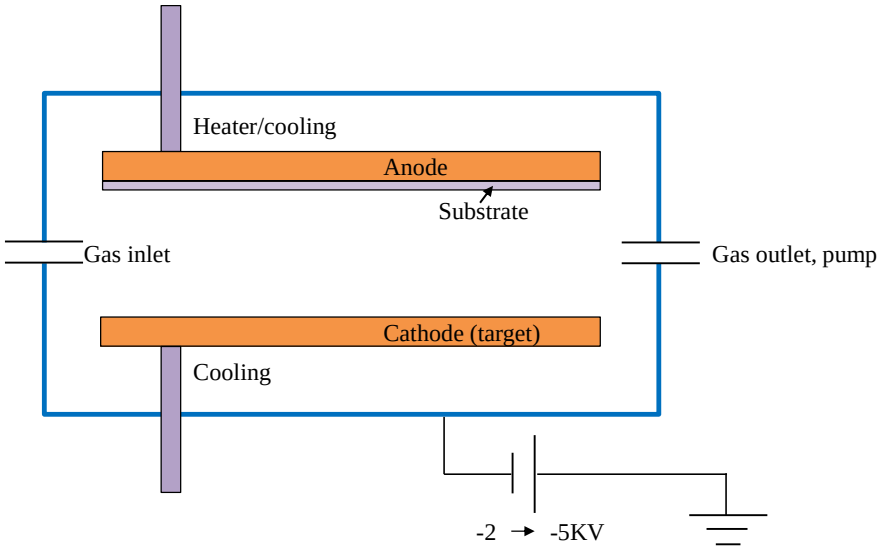

Fig. 2.1 Schematic diagram of DC magnetron sputtering.

DC sputtering is a material deposition process used to coat substrate structures with thin films of different materials. This type of material deposition is achieved by passing a high voltage through an inert, low pressure gas, such as argon, which surrounds a donor and recipient material. The high energy plasma created causes rapidly accelerated ions to strike the donor material, displacing its atoms. The donor atoms then strike and adhere to the recipient material at an atomic level and create a very thin, even film. DC sputtering is capable of extremely accurate and controllable material deposition on a wide variety of substrate surfaces. A ceramic target with a composition ratio of In:Ga:Zn=1:1:1, was utilized for deposition of the active layer in development of the stacked layer on glass

substrate. A 100 nm IGZO was deposited using DC sputtering operating at 150 W and a substrate temperature of 160 °C with a mixed gas of Ar/O_2 (29.4/0.6 sccm) at a deposition pressure of 1 Pa.

2.1.2 Capacitive coupled plasma CVD and inductively coupled plasma CVD technique

PECVD method used in our experiment is one kind of capacitive coupled plasma CVD technique, as shown in Fig. 2.2 (a). PECVD has many advantages, such as low deposition temperature, lower chances of cracks in the deposited layer, good dielectric properties of deposited layer, good step coverage, less temperature dependent, and high quality films. Additional substrate heat is used to improve reaction speed, film density, local crystalline order, and uniformity. In our experiment, SiO_X layer was deposited using PECVD method. The gases, SiH_4 and N_2O, with N_2 as dilution gas, were injected into the plasma reactor chamber. The most important RF plasma-generated reactions are given by (Eq. (2.3), (2.4), (2.5)) [3]

$$SiH_4 + e^{-1} \rightarrow SiH_3 + H^* + e^{-1}; \quad (2.3)$$

$$N_2O + e^{-1} \rightarrow N_2 + O + e^{-1}; \quad (2.4)$$

$$SiH_4 + N_2O + N_2 \rightarrow SiO_X{:}H + H^* + N_2 + H_2 \quad (2.5)$$

A 200-nm-thick SiO_X layer on IGZO was deposited at 170 °C by PECVD.

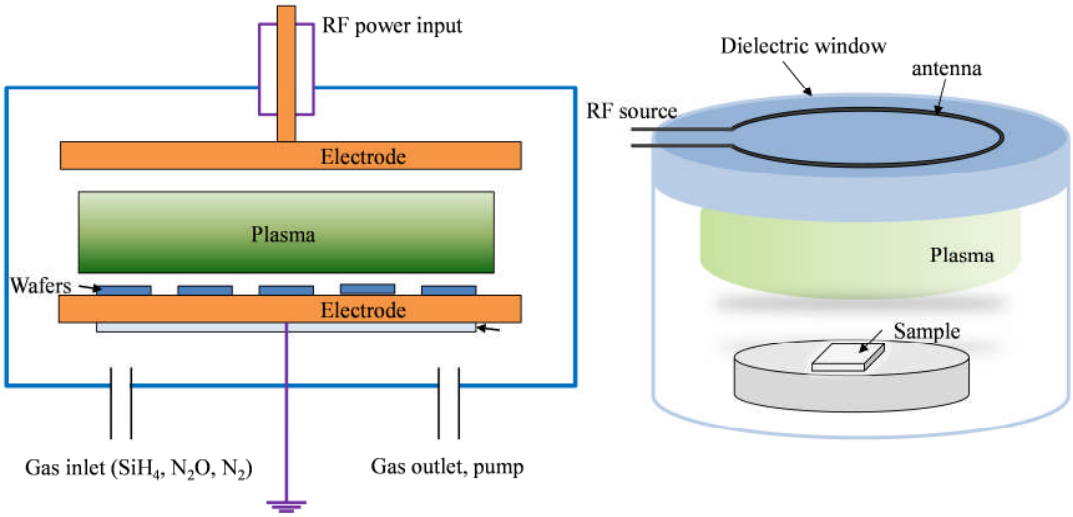

Fig. 2.2 (a) PECVD system, (b) ICP-CVD system (adapted from [4]).

ICP-CVD method has many advantages such as independent control of ion energy and ion current density, plasma in contact with the substrate, low energy ion current during deposition, ion current (plasma density) dependent on ICP power, electrostatic screen (ESS) for purely inductive plasma. So, in our experiment, SiN_X:F layer was deposited using ICP-CVD method, as shown in Fig. 2.2(b) [4]. This system consists of a process chamber in the lower part and an ICP plasma source surrounding by a series of inductive antenna coils in the upper part. The plasma source of this ICP-CVD system includes a radio frequency antenna, a dielectric window and a volume of gas. Inductively coupled plasma is excited by an electric field generated by a transformer from a RF frequency current in antenna coils. The changing magnetic field from this antenna coils induces an electric field in which the plasma electrons are accelerated in the source chamber. Free electrons gain energy by this electromagnetic field and generate ions by collision with neutral gases, thereby generating plasmas. The gases SiF_4 and N_2 were injected into the plasma reactor chamber. The most important RF plasma-generated reactions are given by (Eq. (2.6), (2.7), (2.8))

$$SiF_4 + e^{-1} \rightarrow SiF_3 + F^* + e^{-1}; \quad (2.6)$$

$$N_2 + e^{-1} \rightarrow N^* + e^{-1}; \quad (2.7)$$

$$SiF_4 + N_2 \rightarrow SiN_X{:}F + F^* + F_2 \quad (2.8)$$

A 200 nm SiN_X:F layer was directly deposited on IGZO at 200 °C by ICP-CVD. It should be note that SiO_X:H film contains large number of hydrogen; however, SiN_X:F film used hydrogen-free gas but contains large number of fluorine.

2.2 Characterization techniques

2.2.1 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy works by directing a beam of monoenergetic x-rays photons in the direction of a sample. The photons have certain energy when they hit electrons in the atoms of the sample, and the electrons from the atoms in the sample are then ejected from the atom. The electrons ejected are analyzed in the XPS detector by measuring the electrons kinetic energy, which provides the information to determine the

kind of elements present in the sample. Fig. 2.3 is a schematic representation of the x-ray photoelectron process [5].

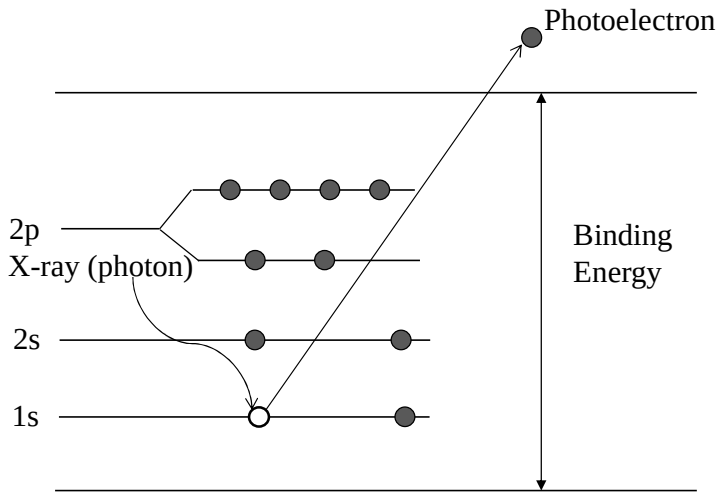

Fig. 2.3 Schematic representation of the X-ray photoelectron process.

The kinetic energy of the ejected electrons is named E_k, and it is determined by the following equation [6].

$$E_k = h\nu - E_b - \phi \qquad (2.6)$$

The binding energy of an electron is represented by E_b, the energy of a photon is given by $h\nu$, where h represents the plank's constant and ν is the frequency of a photon. The work function is represented by the symbol ϕ, which is the minimum energy needed to remove an electron from a solid.

X-ray photoelectron spectroscopy detects the electron energies and identifies the elements and oxidation states of the atoms in a sample. The XPS spectrum shows the number of emitted electrons against their kinetic energy. The XPS method has very important applications for solid surfaces and as nondestructive method of analysis of compounds [7]. The XPS method is based on core electron ejection analysis, which provides a very important qualitative technique since the spectral interface is very small and the XPS peaks for the electrons have good resolution. The peaks on the XPS method have chemical shift that lead to the identification of oxidation states of elements and the chemical composition of the sample.

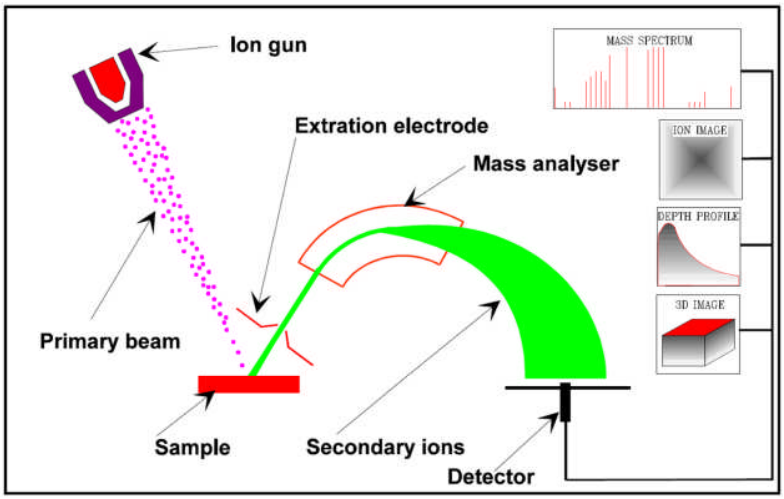

Fig. 2.4 Schematic diagram of SIMS. (adapted from [8]).

2.2.2 Secondary ion mass spectrometry

Secondary ion mass spectrometry is based on the observation that charged particles (secondary Ions) are ejected from a sample surface when bombarded by a primary beam of heavy particles, as shown in Fig. 2.4. Modern SIMS instruments are equipped with a duoplasmatron, a Cs ion source, or a Ga ion source. In our experiment, the Cs ion source was used. Cs ion beams were able to enhance the yield of electronegative elements within the target. In general, Cs beams sputter material more effectively because of their greater mass. The primary ions generated by the ion source are passed to the sample via the primary column. A typical column consists of a mass filter, apertures, lenses and deflection plates. Their function is to filter, focus, shape, position and raster the primary beam. Secondary ions are formed at the sample surface after bombardment by the primary beam. These secondary ions are immediately removed by an extraction, or immersion lens. After the secondary ions have been extracted from the sample surface by the immersion lens, they are transferred by a second electrostatic (transfer) lens into the mass spectrometer. Secondary ions generated during the sputtering process have a wide range of energies. As an ion beam passes through a magnetic field, the ions are acted on by a force at right angles to both the direction of motion of the ion and to the direction of the magnetic field. The magnitude of the magnetic field required to deflect the ion species is given by the equation:

$$\frac{m}{q} = \frac{B^2}{2V} \times r^2 \tag{2.7}$$

m/q is mass to charge ratio, B is strength of the magnetic field. V is the ion accelerating voltage. r is the radium of curvature of the magnetic field. The ion required the following eq. (2.7) would be collected. Finally, mass spectrometers used secondary ion detectors to show mass spectrum, ion image, depth profile and 3D image [8].

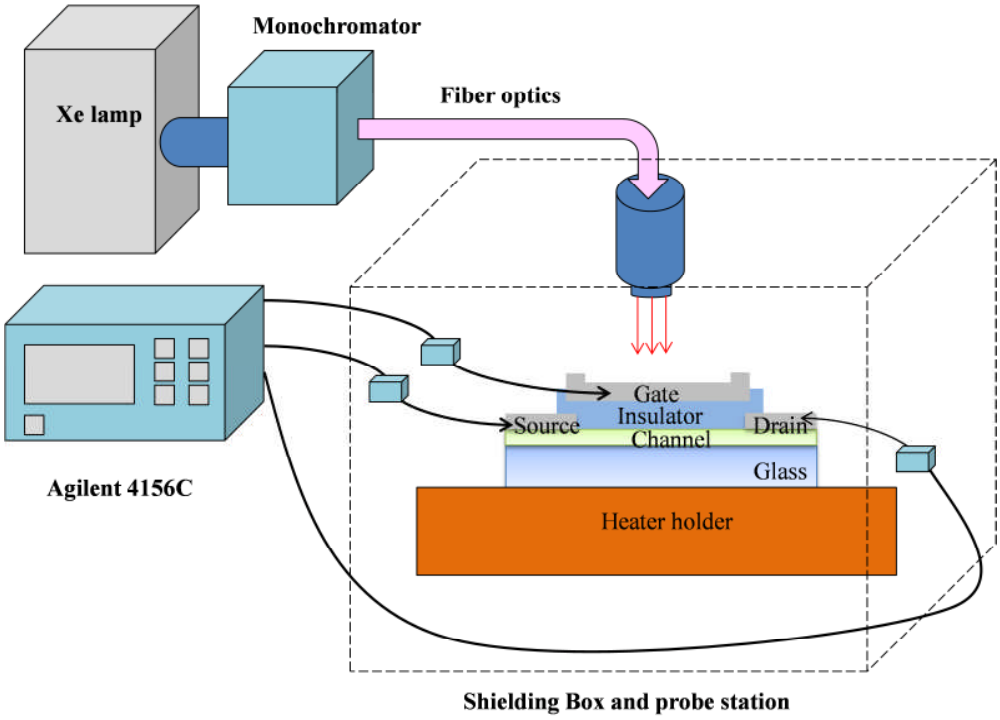

Fig. 2.5 Schematic diagram of the experimental equipment utilized in the study.

2.2.3 TFTs evaluation system

Stability tests were carried out with the system shown in Fig. 2.5. Test devices were isolated from the external light by using the shielding box. Agilent 4155C semiconductor parameter analyzer and a probe station system were utilized for electrical measurements and stress tests. Monochromatic light was achieved by combining a Xe lamp and a monochromator. The wavelengths of the light for illumination were changed from 630 nm and 400 nm. The power density of each light was set to be 0.2 mW/cm^2. The stress conditions were split based on combination of the polarity of the DC gate bias and the wavelength of the incident light. The maximum time duration for each stress condition

was 10^4 second. The holder platform of the sample connected with the temperature adjustment equipment to carry out the temperature stress. Transfer characteristics were measured with/without light illumination on a logarithmic time scale.

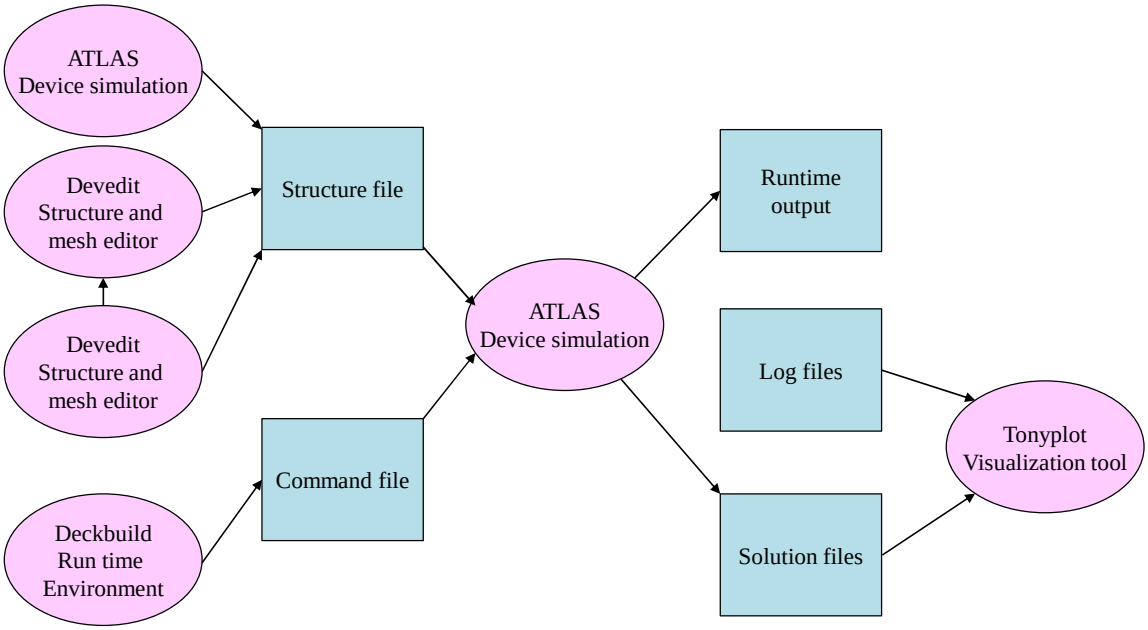

Fig. 2.6 Schematic diagram of ATLAS inputs and outputs.

2.2.4 Device simulation (ATLAS)

ATLAS is a 2D and 3D device simulation framework, which can give insights into the internal characteristics of semiconductor device. A diagram of ATLAS inputs and outputs is shown in Fig. 2.6. Device structure file can be built using ATLAS, DevEdit and ATHENA. Input files of structure file and command file imported to ATLAS, after simulation, output files of log files and solution files can be visualized by TonyPlot [9]. The elements of ATLAS input file are shown in Fig. 2.7. The input file of ATLAS can be divided into 5 groups including structure specification, material models specification, numerical models specification, solution specification and results analysis [9]. The corresponding statements of each group are shown on the right side of Fig. 2.7. TFT is an ATLAS module that simulates disordered material systems. TFT 2D is an advanced device technology simulator equipped with physical models and specialized numerical techniques required to simulate amorphous or polysilicon devices, focusing on defects

and defect states. The accurate modeling of these defects and the density of defect states is critical for accurate predictive software. The properties of the defect states in the material's band gap can be easily adjusted by specifying activation energy, and capturing cross-sections or lifetimes for electrons and holes. The distribution of defects is specified by the user as a function of energy. Users can easily modify trap definitions to specify material characterizations. The TFT 2D module models the electrical effects of these properties through accurate mathematical and experimental proven default equations. Grain boundary and grain boundary effects can also be simulated and analyzed [10].

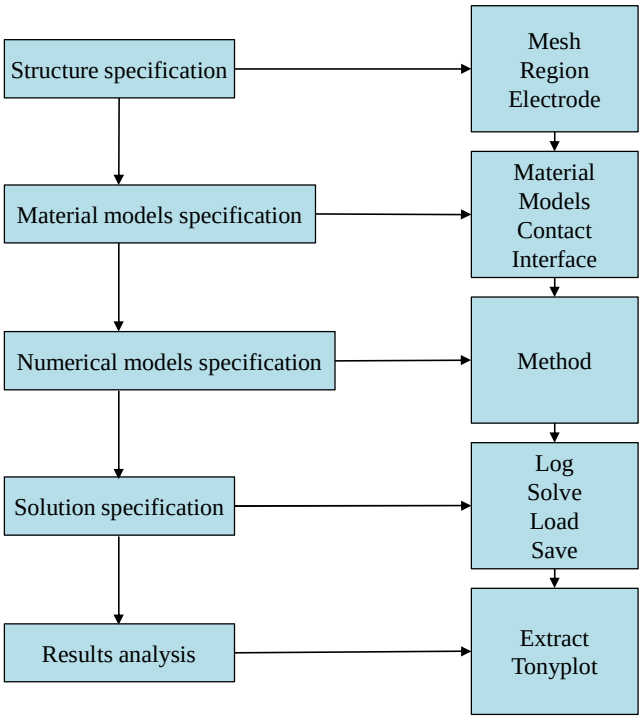

Fig. 2.7 Elements of ATLAS input.

2.3 Reference

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[10] ATLAS Device Simulation Software User’s Manual (Silvaco, Santa Clara, CA, 2012).

Chapter 3

Study on density of states of a-In-X-Zn-O (X=Ga, Sn) TFTs using device simulation

3.1 Introduction

Recently, oxide thin-film transistors have attracted considerable attention for use in next generation large-area flat panel displays, due to their superior electrical properties, in particular high mobility, steep *S*, and good electrical stability [1-3] as compared with a-Si:H TFTs. In general, the *S* value is an indicator of the maximum area density of state (N_t) including the interfacial traps in channel/insulator and the semiconductor bulk traps. The N_t value can be extracted from following equation [4]:

$$N_t = \left(\frac{S \log e}{kT/q} - 1 \right) \frac{C_i}{q} \tag{3.1}$$

Where *q* is the electron charge and *k* is the Boltzmann constant. The *S* value reflects the density of subgap traps, and knowledge of this density subgap DOS is important for improving the TFT characteristics. Fig. 3.1 shows a schematic electronic structure of a-IGZO. A-IGZO has tail states below the conduction band minimum (CBM) and above the valence band maximum (VBM), and their energy dependence follows the Urbach law as $D_{sg}(E)$ / exp (E/E_u) (E_u is called the Urbach energy). The typical E_u is about 13-150 meV for the conduction band tail. Fung *et al.* [5] reported that the tail states below CBM originated from the disorder of metal ion *s*-bands, while the oxygen *p*-band disorder mainly contributed to the tail states above VBM. As-deposited a-IGZO film (deposition at RT) has extra gap states 0.2 eV below CBM, which is related to hysteresis in capacitance voltage characteristics and TFT characteristics [6]. In additional, hard X-ray photoemission spectroscopy (HX-PES) revealed that high-density electron traps exist just above VBM with the energy range of 1.5 eV [7], which could be the reason why a-IGZO TFTs have never operated in p-channel TFT mode [8].

The influence of DOS for a-IGZO TFTs on electrical properties was investigated in many studies. Fung *et al.* [5] reported that higher acceptor-like tail states near CBM induced a significant decrease in TFT drain current. The movement of Fermi level (E_F)

toward conduction band (E_C) is smaller for TFT with higher acceptor-like tail states near CBM, and it takes a larger gate voltage to reach the same level of E_C−E_F. As a result, the maximum achievable band bending decreases, lowering the free electron concentration in the conducting channel and reducing the drain current. Furthermore, it has been reported that the Gaussian-distributed acceptor-like states exist near valence band (E_V) of IGZO TFT [9]. Kamiya *et al.* investigated the influence of deep level acceptor traps [9]. The variations in the deep Gaussian acceptor-like states have the effect of shifting the turn-on voltage of the transfer curve, while the *S* and on current stay nearly unchanged. In addition, a change of deep donor-like states does not affect DC *I-V* characteristics. The deep states of tail states above VBM and deep donor states in n-channel AOS TFTs are filled with electrons under most practical operation conditions since E_F is quite close to E_C even under a thermal equilibrium. It means that deep states are electrically neutral, and therefore, a change in deep states does not affect DC *I–V* characteristics [10].

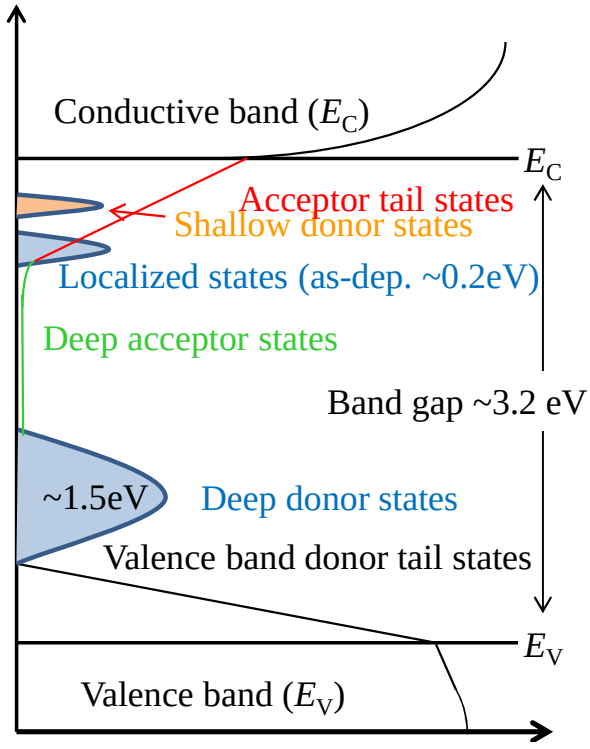

Fig. 3.1 Schematic models of subgap DOS in a-IGZO. (Ref. Sci. Technol. Adv. Mat., 11,044305 (2010))

3.2 Influence of front- and back-channel interface traps on the electrical properties of oxide TFTs with different channel thicknesses

3.2.1 Introduction

Since electrical properties are highly dependent on the density of localized states, there have been many studies on the effects of DOS in oxide semiconductors on the electrical properties of the TFTs [5,9,11-13]. So far, two kinds of DOS model have been proposed to understand the electrical characteristics of oxide TFTs with different channel thicknesses. The first is a constant DOS model across the entire channel regardless of the channel thickness [4,11]. In this model, degradation of *S* value is observed as channel thickness increased because total number of the traps increased with increasing channel thickness. The second model is a thickness-dependent DOS model. In this model, total DOS increases with decreasing channel thickness due to the increase of disorders in the amorphous phase; therefore, the *S* value of the TFT deteriorates with decreasing channel thickness [14].

Our a-ITZO TFTs shown in Figs. 3.2 and 3.3 exhibited superior electrical properties such as steep *S* characteristics and high mobility. In addition, the *S* value of the ITZO TFTs improved with increasing channel thickness, which can be explained by the second DOS model. Many extraction techniques of DOS for oxide TFT have been developed [14-16]. The extracted DOS consists of in-film traps and insulator-interface traps located at a front- or back-channel interface. Most previous works on the DOS of a-IGZO TFTs considered bulk DOS and front-channel interface traps. However, for bottom-gate oxide TFTs with an etch-stopper and/or passivation layer, traps at back-channel interface should be considered because the traps will be formed not only in the bulk region but also in the back-channel region of oxide semiconductor due to ion bombardment, hydrogen diffusion, and the redox reaction of the oxide semiconductor during ES deposition [17-19]. However, the difference between the influence of front- and back- channel interface traps on the electrical properties of oxide TFTs has rarely been studied to date.

In this study, the effect of front- and back-channel interface traps on the electrical properties of a-ITZO TFTs with different channel thicknesses was investigated, by means of 2D device simulation. It was confirmed that not only front-channel interface traps but

also back-channel interface traps are important factors of S and V_{on} for thinner channel TFTs in order to achieve high performance oxide TFTs.

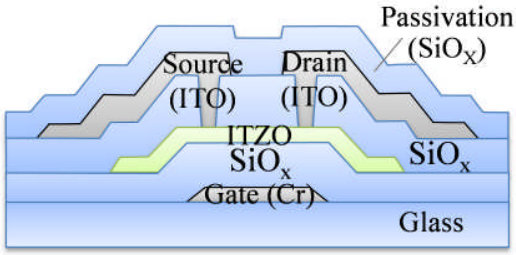

Fig. 3.2 Schematic cross-sectional view of the ITZO TFT.

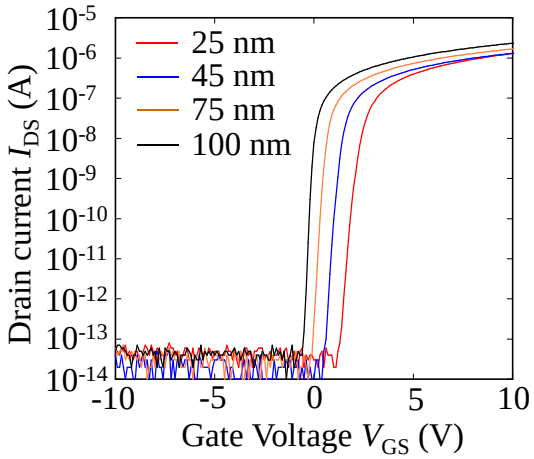

Fig. 3.3 Transfer characteristics of the ITZO TFTs with different T_{ITZO}.

3.2.2 Experimental procedure

In this study, a bottom-gate ITZO TFT with SiO_X etch-stopper and SiO_X passivation was used as a motif device, as shown in Fig. 3.2. A gate insulator of SiO_X (150 nm) was deposited at 350 °C by PE-CVD. The ITZO layer was then deposited at 160 °C by direct current sputtering with a mixed gas of Ar/O_2 (15/15 sccm) at a deposition pressure of 1 Pa. The thickness of the channel layer of ITZO (T_{ITZO}) was between 25 and 100 nm. After definition of an ITZO channel, an etch-stopper was formed by SiO_X film (200 nm), which was deposited by PE-CVD at 170 °C. The source and drain electrodes were formed by indium-tin-oxide (ITO) via contact holes. The SiO_X passivation (200 nm) was further deposited by PE-CVD. Finally, the ITZO TFTs were annealed in N_2 ambient at 350 °C

for 1h. The channel length (L) and width (W) of the TFTs were 20 and 50 μm, respectively.

3.2.3 Results and discussion

3.2.3.1 Electrical properties of ITZO TFT with different T_{ITZO}

The experimental transfer characteristics (I_{DS}-V_{GS}) of ITZO TFTs with different T_{ITZO} are shown in Fig. 3.3. Transfer characteristics were measured at a V_{DS} of 0.1 V. The electrical properties are summarized in Table 3.1. Field-effect mobility (μ) was extracted from the transconductance at a drain current in the linear region using the following equation:

$$\mu = \frac{Lg_m}{WC_iV_{DS}} \tag{3.7}$$

where C_i and g_m were the gate capacitance per unit area and the transconductance, respectively. V_{on} was defined by V_{GS} at a drain current (I_{DS}) of 1 pA. The hysteresis (V_H) of transfer curves was defined in a clockwise direction by the difference in V_{on} between forward and reverse V_{GS} sweeps. S was calculated from V_{GS}, which requires an increase in I_{DS} from 10 to 100 pA. The ITZO TFTs show high field effect mobility of ~30 $cm^2V^{-1}s^{-1}$. The experimental results show a gradually negative shift in transfer curves and decrease in S value with increasing T_{ITZO}. In the following section, the ITZO TFTs simulation model was set up based on the IGZO TFTs model to analyze the channel thickness-dependent S property.

Table 3.1 Electrical properties of ITZO TFTs with different T_{ITZO}.

Channel layer thickness (nm)	25	45	75	100
mobility (μ) ($cm^2V^{-1}s^{-1}$)	35.3	37.9	33.2	46.3
V_{on} (V_{GS} @ I_{DS} = 1pA (V))	1.5	0.7	0.0	-0.5
Hysteresis (@ V_{on} (V))	0.03	0.12	0.08	0.02
S (V/dec.)	0.19	0.17	0.14	0.09

3.2.3.2 Establishment of simulation model

A 2D inverted-staggered bottom-gate a-IGZO TFT structure used for numerical simulation is shown in Fig. 3.4, which is designed to match the actual TFT used in this

chapter. The structure consists of a 45 nm thick a-IGZO active layer and a 150 nm thick thermal SiO_2 gate insulator layer. It should be mentioned that the 2D simulation only calculates the distribution of physical properties along the channel length (L). An ideal, uniform distribution is assumed along the channel width (W). In this study, the ratio of W/L of TFT is 50/20. The homogeneous Neumann boundary condition [20] is applied to the back-channel surface of the a-IGZO layer. Such boundary condition prevents carriers from flowing outside of the back-channel surface and ensures that the current only flows in/out of the device through S/D contacts during simulation. In addition, since the degenerate conduction might occur in the a-IGZO TFT [21,22] the fermi-dirac statistic is used in numerical simulation. Contacts between S/D electrodes and the a-IGZO layer were either assigned as schottky in nature. For the Schottky model, the S/D metal work function is 4.44 eV. For a-IGZO with an atomic ratio of ln:Ga:Zn =1:1:1, the electron affinity of a-IGZO was calculated to be 4.16 eV. We set the electron band mobility n=15 $cm^2V^{-1}s^{-1}$ to be the maximum mobility calculated from TFT transconductance. Most metal oxides have a strong localization behavior of a positive hole at the valence band edge to a single oxygen atom that prevents the hole from freely moving within the crystal lattice [23]. In this study, the hole band mobility was chosen to be 0.01 cm^2/Vs. We also developed the DOS model for a-IGZO based on several published results. Takagi et al. [24] extracted the conduction band effective mass (m_c) to be ~0.34 m_e (m_e is the mass of free electron) in their early work on a-IGZO. We further calculated the effective conduction band DOS (Nc) to be 5×10^{18} cm^{-3} at room temperature using equation (3.2):

$$N_c = 2\left(\frac{2\pi m_c kT}{h^2}\right)^{3/2} \quad (3.2)$$

Where kT=25 meV and h is the Planck constant [25]. The key simulation parameters of IGZO are listed in Table 3.2.

Table 3.2 Key simulation parameters in a-IGZO TFTs.

Name	Value
Effective conduction band DOS (cm^{-3})	5×10^{18}
Effective valence band DOS (cm^{-3})	4.9×10^{18}
Bandgap (eV)	3.05
electronic affinity (eV)	4.16
Permittivity	12
Electron mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	13
Hole mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	0.01

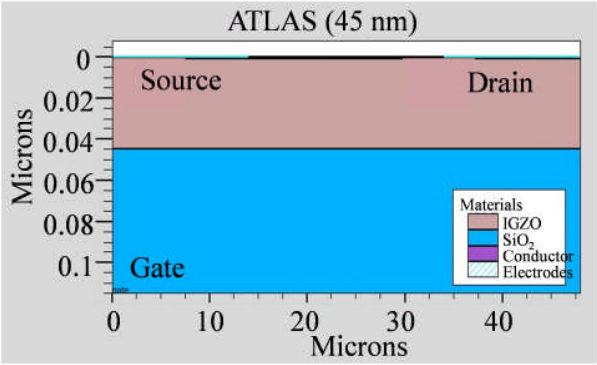

Fig. 3.4 Simulation structure of IGZO (ITZO) TFTs.

So far, several bulk DOS models for IGZO TFT by 2D device simulation have been proposed [5,9,11,12,26-28]. Several published studies on IGZO TFT [5,9,12,26] reported that bulk DOS was composed of acceptor-like conduction band tail states (g_{CBa}), Gaussian distributed acceptor-like states (g_{Ga}), donor-like valence band tail states (g_{VBd}), and Gaussian distributed donor-like states (g_{Gd}) for IGZO TFT. These states are expressed as a function of energy (E) by the following equations:

$$g_{CBa} = g_{ta}\exp[(E - E_C)/E_a] \tag{3.3}$$

$$g_{Ga} = g_a\exp[-(E - \lambda_a)^2/{\sigma_a}^2] \tag{3.4}$$

$$g_{VBd} = g_{td}\exp[(E_V - E)/E_d] \tag{3.5}$$

$$g_{Gd} = g_d\exp[-(E - \lambda_d)^2/{\sigma_d}^2] \tag{3.6}$$

where E_C and E_V are conduction and valence band edge energies; g_{ta} and g_{td} are densities of acceptor-like and donor-like tail states at $E = E_C$ and $E = E_V$, respectively; E_a and E_d are characteristic slopes of conduction and valence band tail states, respectively; g_a, λ_a, and σ_a are the Gaussian-distributed acceptor-like states peak value, the mean energy, and standard deviation of states, respectively; and g_d, λ_d, and σ_d are the Gaussian-distributed donor-like states peak value, the mean energy, and standard deviation of states, respectively. λ_a is fixed at E_C to represent a monotonously decreasing deep gap state. The bulk DOS of a-IGZO model used in the device simulation is shown in Fig. 3.5. All the parameters extracted from a-IGZO TFTs used in this numerical simulation are listed in Table 3.3. Transfer characteristics were measured at a drain voltage (V_{DS}) of 0.1 V. The electrical properties of a-IGZO are summarized in Table 3.4. Fig. 3.6 shows the

experimental and simulated transfer characteristics of the IGZO TFTs. The simulated results were consistent with the experimental transfer characteristics of IGZO TFTs.

Table 3.3 Extracted values of DOS of IGZO TFT.

Parameter	Value
g_{ta}	2.2×10^{19} $cm^{-3}eV^{-1}$
E_a	0.07 eV
g_{td}	1.55×10^{20} $cm^{-3}eV^{-1}$
E_d	0.12 eV
g_d	3×10^{16} $cm^{-3}eV^{-1}$
λ_d	2.68 eV
σ_d	0.08 eV
g_a	4.5×10^{17} $cm^{-3}eV^{-1}$
λ_a	0.225 eV
σ_a	0.048 eV

Table 3.4 Electrical properties of IGZO TFTs.

Parameters	Value
mobility (μ) ($cm^2V^{-1}s^{-1}$)	12.52
V_{on} (V_{GS} @ I_{DS} = 1pA (V))	0.98
Hysteresis (V) (V_{GS} @ I_{DS} = 1pA (V))	0.42
S (V/dec.)	0.49

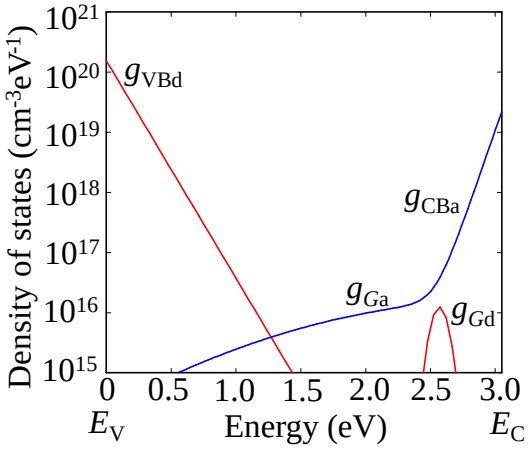

Fig. 3.5 Bulk DOS of a-IGZO model used in the device simulation.

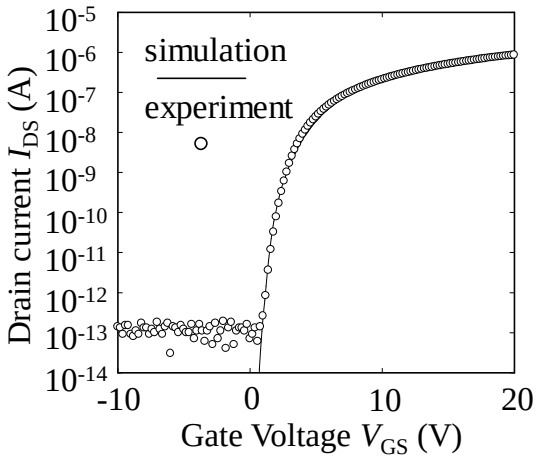

Fig 3.6 Simulated and experimental I_{DS}-V_{GS} characteristics of IGZO TFTs.

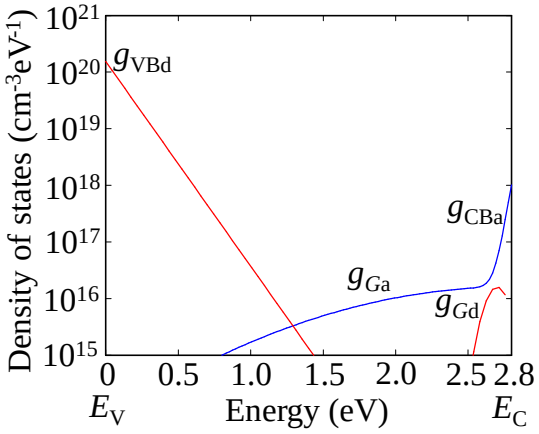

Fig. 3.7 Bulk DOS of a-ITZO model used in the device simulation.

In this study, the conduction band effective mass (m_c) of a-ITZO is extracted to be ~0.36 m_e [29], which is almost the same as that of a-IGZO (~0.34 m_e). Subsequently, the effective conduction band DOS is further calculated to be 5.46×10^{18} cm^{-3}. Based on the maximum mobility calculated from TFT transconductance, the electron band mobility was set to be 35 cm^2/Vs in the simulation. The electron concentration and the difference between the work function of ITO and the electron affinity of a-ITZO may be fine adjusted to further improve the fitting. In addition, we used bulk DOS of a-ITZO based on simulation model of a-IGZO. M. Li [19] and X. Li [30] reported that SiO_X passivation or (etch-stopper layer) deposition introduced hydrogen into the oxide semiconductor.

Since hydrogen in oxide semiconductor introduced shallow donor level near E_C, we assume g_{Gd} at E_C - E of 0.1 eV [5]. The energy distribution of bulk DOS used in this simulation is shown in Fig. 3.7. All the parameters extracted from a-ITZO TFTs used in this numerical simulation are listed in Table 3.5.

Table 3.5 Extracted values of DOS of ITZO TFT.

Bulk		Channel interface traps	
Parameter	Value	Parameter	Value
g_{ta}	1×10^{18} cm^{-3}eV^{-1}	N_{abk}	3×10^{11} cm^{-2}eV^{-1}
E_a	0.03 eV	N_{af}	1.4×10^{11} cm^{-2}eV^{-1}
g_{td}	1.55×10^{20} cm^{-3}eV^{-1}		
E_d	0.12 eV		
g_d	1.6×10^{16} cm^{-3}eV^{-1}		
λ_d	2.7 eV		
σ_d	0.1 eV		
g_a	1.6×10^{16} cm^{-3}eV^{-1}		
λ_a	2.8 eV		
σ_a	1.2 eV		

3.2.3.3 Degradation mechanism of S for a-ITZO TFTs with decreasing T_{ITZO}

In essence, degradation in S value with decreasing channel thickness of the a-ITZO TFTs can be attributed to either an increase in bulk defect density of the semiconductor itself, or the stronger influence of localized traps at the front- or back-channel interface [14,31,32]. These two factors both induced the increase of subgap DOS as the channel thickness decreased. To analyze the channel thickness-dependent S properties of amorphous oxide-based semiconductor TFTs, two mechanisms have been proposed to account for the increase of S as channel layer thickness decreases.

The former model shows an increase in bulk DOS with a corresponding decrease in T_{ITZO} due to the increase of disorders in an amorphous structure [14]. Ordering of atomic structure will be superior with relatively longer processing time. This is consistent with the idea that film quality is improved when film thickness increases. Kamiya *et al.* [9] reported that the variations of the deep Gaussian acceptor-like states had a major effect on positive shift of V_{on} of the transfer curve, while the S value and on-current remained nearly constant. In addition, a change of deep donor-like states would not affect DC I-V characteristics because the deep donor-like states are electrically neutral. Therefore, the main factor influencing S value is the localized acceptor-like tail states, which become

slightly larger with decreasing thickness due to the disorder in the ITZO film.

The latter model shows a stronger influence of localized interface traps at front- or back-channel interface as T_{ITZO} decreases. However, the difference between the influences of front- and back-channel interface traps on electrical properties of oxide TFTs has rarely been studied to date. In this study, the influences of localized front- and back-channel interface traps on the electrical properties of oxide TFTs are investigated by 2D device simulation. In this simulation, since localized traps at front- or back-channel interface trap have a stronger influence on electrical properties than the bulk DOS in the channel, bulk DOS in the channel is assumed to be constant with T_{ITZO}, meaning that the quality of the sputtered ITZO channel layer was not affected by T_{ITZO} [11,12,33].

3.2.3.4 Effect of front- and back-channel interface traps on S and V_{on}

In addition to the bulk DOS, the localized traps at front- or back-channel interface are introduced. For bottom-gate oxide TFTs with an etch-stopper and passivation layer, the property of the back-channel is inferior to that of the front-channel, which has a higher density of electron traps than the front-channel due to the chemical etching and plasma treatment during the TFT fabrication [34]. Nomura *et al.* [18] reported the existence of high-density deep subgap defects in a back-channel region. What is more, it is difficult to estimate the energy distribution of the deep subgap defects; thus, the type and distribution of interface traps were assumed as acceptor-like states and constant in the bandgap, respectively. The N_t values is calculated in equation (3.1) to be about 2.62×10^{11} $cm^{-2}eV^{-1}$ for the TFT with 45nm ITZO film. In our simulation, the total number of bulk traps and front-channel interface traps (N_{af}) almost equal the calculated value. Using the same bulk traps, through optimized fitting to the experimental transfer, we get the back-channel interface traps (N_{abk}). The traps at the channel/gate-insulator interface and channel/etch-stopper interface are named as front-channel interface traps (N_{af}) and back-channel interface traps (N_{abk}), respectively. Bulk DOS with front-channel interface traps ($N_{af} = 1.4 \times 10^{11}$ $cm^{-2}eV^{-1}$) and the bulk DOS with back-channel interface traps ($N_{abk} = 3 \times 10^{11}$ $cm^{-2}eV^{-1}$) are respectively named as model 1 and model 2. The DOS parameters of ITZO TFTs used in the device simulation are listed in Table 3.5. Both models can effectively reproduce the experimental transfer curve of the ITZO TFT with T_{ITZO} of 45 nm. Based

on these models, the influence of front- and back-channel interface traps on the thickness-dependent performance variation of oxide TFT was investigated.

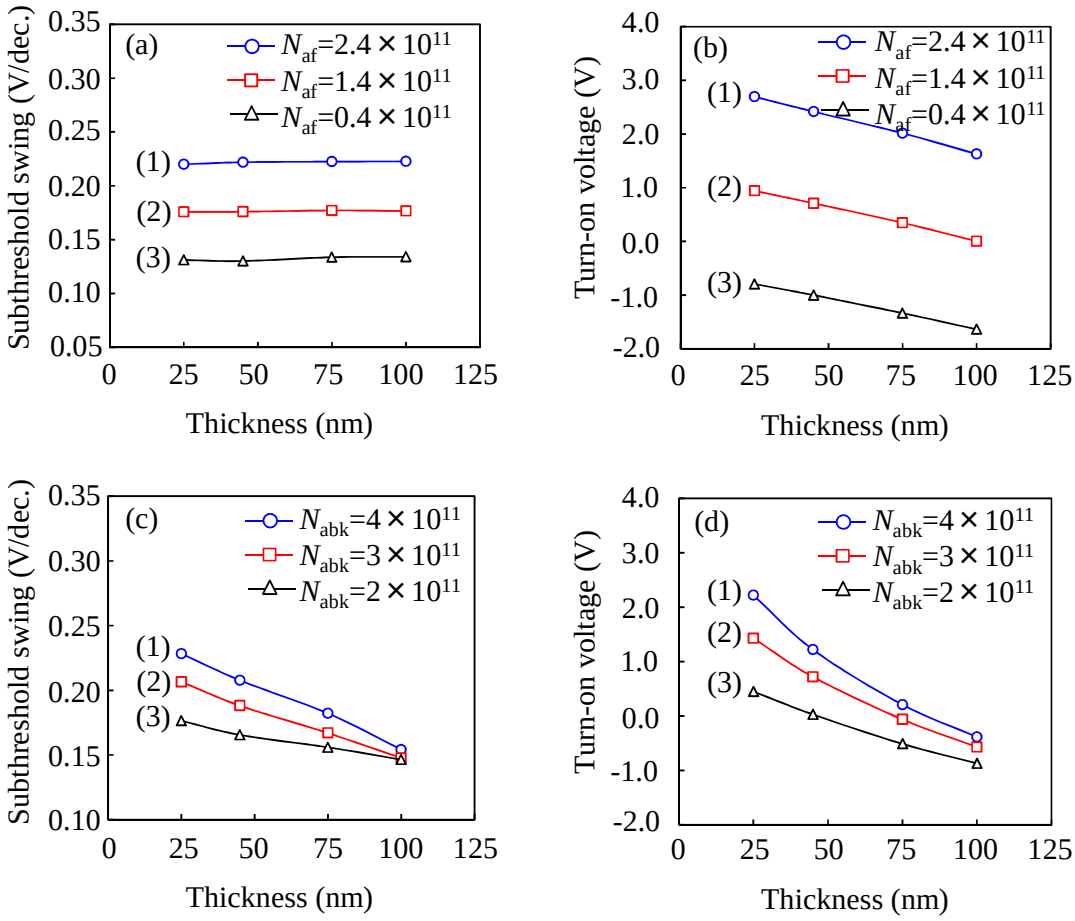

Fig. 3.8 Effect of changing the front-channel interface traps N_{af} ($cm^{-2}eV^{-1}$) on (a) S and (b) V_{on} of ITZO TFTs with different T_{ITZO}. Effect of changing the back-channel interface traps N_{abk} ($cm^{-2}eV^{-1}$) on (c) S and (d) V_{on} of ITZO TFTs with different T_{ITZO}.

Fig. 3.8(a) and 3.8(b) show the S value and V_{on} of the ITZO TFTs respectively with different N_{af} as a function of T_{ITZO}.

Curve (2) in Figs. 3.8(a) and 3.8(b) shows the thickness dependence of the S and V_{on} of the ITZO TFTs using DOS model 1 with the N_{af} of 1.4 × 10^{11} $cm^{-2}eV^{-1}$, respectively. It was found that the S value barely changed by changing the T_{ITZO}. On the other hand, the V_{on} shifted about 1 V in the positive V_{GS} direction as the T_{ITZO} decreased from 100 to 25 nm. To further analyze the above mentioned results, the N_{af} was varied from 2.4 × 10^{11} to 0.4 × 10^{11} $cm^{-2}eV^{-1}$. When N_{af} increased or decreased by 1 × 10^{11} $cm^{-2}eV^{-1}$, S value and

V_{on} increased or decreased correspondingly by about 0.5 V/dec. and 2 V, regardless of the T_{ITZO}. These results indicate that the influence of N_{af} on S and V_{on} is much larger than the bulk DOS. Moreover, the N_{af} mainly influences carrier density near the channel/gate-insulator interface, resulting in the change of S and V_{on}.

Fig. 3.8(c) and 3.8(d) show the S value and V_{on} of the ITZO TFTs using model 2 with different N_{abk} as a function of T_{ITZO}.

In contrast to Fig. 3.8(a), it was found that the S value with the N_{abk} of 3×10^{11} $cm^{-2}eV^{-1}$ degraded from 0.15 to 0.21 V/dec. when the T_{ITZO} decreased from 100 to 25 nm. It is noted that the thickness dependence of the S value became greater as the N_{abk} increased. The V_{on} also exhibited a positive shift with increasing N_{abk} and decreasing T_{ITZO}. These results indicate that the influence of the N_{abk} on S and V_{on} becomes dominant especially for thinner T_{ITZO}.

These results can be explained by considering the concept of the screening length λ of the oxide semiconductor. The screening length λ is defined by $\sqrt{\varepsilon_s/qN_T}$ [35], which is the distance over which energy band bending occurs in order to "screen" the applied gate voltage. Here ε_s and N_T are permittivity of semiconductor and intrinsic bulk trap density. The screening length is estimated to be in the range of 78-81 nm [36,37]. As the channel layer is thinner than λ, the change in the gate voltage causes band bending and the movement of the Fermi level (E_F) simultaneously; thus, negatively charged acceptor-like N_{abk} increases due to electron trapping. E_F at back-channel (ΔE_{back}) of the TFT with thinner T_{ITZO} shifts upward more than with thicker T_{ITZO}; this means that N_{abk} traps more electrons for thinner T_{ITZO} TFT. Thus, the increment of carrier density for thinner ITZO TFT is smaller than for the thicker T_{ITZO} TFT, resulting in the deterioration of S along with decreasing T_{ITZO}. For 100nm channel layer TFT, since T_{ITZO} is larger than λ, the E_F near the back-channel region is pinned even though the gate voltage varies. In other words, N_{abk} does not influence the carrier density in the front-channel region, so the S value is not changed by N_{abk} for the TFT with T_{ITZO} of 100 nm. In the case of thinner T_{ITZO} TFT ($T_{ITZO} < \lambda$), N_{abk} significantly influences the S value and V_{on} of the TFT.

These simulation results indicate that back-channel interface traps should be considered as a means to achieve high performance oxide TFTs with thinner channel.

3.2.4 Conclusions

We investigated the electrical properties of bottom-gate a-ITZO TFTs with different channel thicknesses. Superior performances were observed, in particular steep S and high mobility. The tendency for the S of a-ITZO TFTs to increase with decreasing T_{ITZO} was examined using two degradation mechanisms. One mechanism is the higher density of localized acceptor-like tail states in thinner a-ITZO film. The other is a stronger influence of the localized interface traps due to the decrease of channel thickness. The influence of localized interface traps on the S and V_{on} with different thicknesses has been discussed in detail, by means of device simulation. It was found that S degraded and V_{on} positive shifted when N_{af} or N_{abk} increased. The influence of N_{af} was stronger than that of N_{abk}; however, thickness dependence of variation of S and V_{on} showed a different tendency when N_{af} and N_{abk} varied. The influence of N_{af} on S was independent of T_{ITZO}; furthermore, variations of N_{af} on S and V_{on} were hardly dependent on T_{ITZO} when N_{af} varied. On the other hand, influence of N_{abk} on S and V_{on} became significant when T_{ITZO} decreased, these phenomena that can be explained by considering the screening length. Simulation results confirmed that not only N_{af} but also N_{abk} are important factors of S and V_{on} for thinner channel TFTs in work to achieve high performance oxide TFTs.

3.3 Conclusions

The DOS model of In-X-Zn-O (X= Ga, Sn) TFTs was set up using device simulation. The influence of DOS on electrical properties of bottom-gate a-IGZO and ITZO TFTs was studied. The difference between the influence of front- and back- channel interface traps on the electrical properties of oxide TFTs was discussed in detail, by means of device simulation. It was confirmed that not only N_{af} but also N_{abk} are important factors of S and V_{on} to achieve high performance thinner oxide TFT. The proposed thickness-dependent analysis method for front- and back-channel interface traps could become a useful tool for optimization of the fabrication process of oxide TFTs.

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Chapter 4

High stable fluorine-passivated IGZO TFTs through long time annealing

4.1 Introduction

4.1.1 Defects passivation methods to reduce the density of states

a-IGZO is widely considered to be a promising channel material for TFT applications [1-4]. However, as the initial performance and stabilities of a-IGZO TFTS still need further improvements, reduction and/or passivation of DOS may be an effective method to improve performance and stabilities for oxide TFTs. Reported methods for the reduction of traps in oxide TFTs included a process for enhancing oxidation such as atmospheric-pressure or high-pressure O_2, O_3, and/or H_2O annealing [5-8]. Trap passivation is a method for non-activation of defects, including hydrogen and fluorine (F) termination methods. Hydrogenation is a technique employed to passivate defects [9,10]; however, H is known as a shallow donor [11] and is not expected to be thermally stable in a-IGZO. Since the ionic radius of F is close to that of oxygen, F is a candidate element for passivation of oxygen deficiencies and/or weakly bonded oxygen in oxide semiconductors. Recently, ion implantations of F and CF_4 or CHF_3 plasma immersion have been employed to terminate defects and improve the electrical performance of ZnO and IGZO TFTs [12-14]. In addition, it was also reported that a SiN_X:F gate insulator (GI) is effective for improving the positive bias and temperature stress (PBTS) stability of IGZO TFTs owing to the improvement of the GI/IGZO interface quality [15]. So we propose a novel F passivation method of oxygen deficiencies using SiN_X:F as a fluorine source in order to achieve high performance and highly stable oxide TFTs.

4.1.2 Analysis the feasibility of fluorine passivation methods

To investigate the effects of fluorine in IGZO, the electrical and chemical properties of SiN_X:F/IGZO stacked layers were analyzed. Two kinds of stacked layer of SiN_X:F/IGZO/Glass and SiO_X/IGZO/Glass were fabricated, as shown in Fig. 4.1. A ceramic target with a composition ratio of In:Ga:Zn=1:1:1 was utilized for deposition of the IGZO layer in development of the stacked layer on glass substrate. A 100 nm IGZO

was deposited using DC reactive sputtering operating at 150 W and a substrate temperature of 160 °C with a mixed gas of Ar/O_2 (29.4/0.6 sccm) at a deposition pressure of 1 Pa. In our experiment, a 200-nm-thick SiO_X layer on IGZO was deposited at 170 °C by PE-CVD with a mixed gas of $SiH_4/N_2O/N_2$ [16]. SiN_X:F layer was deposited using the ICP-CVD method. A 200 nm SiN_X:F layer was directly deposited on the IGZO at 200 °C by ICP-CVD with a mixed gas of SiF_4/N_2.

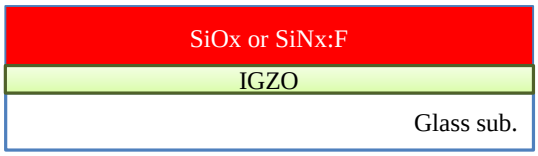


Fig. 4.1 Schematic of stacked layer.

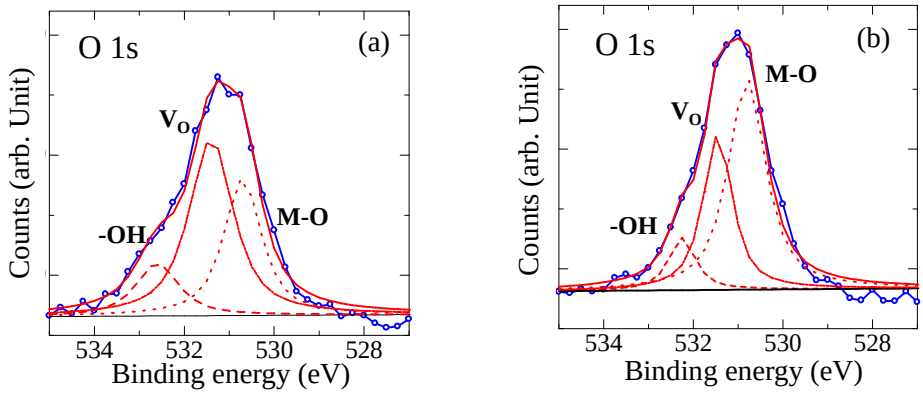


Fig. 4.2 O1s XPS spectra in IGZO films for SiO_X/IGZO stack films, (a) as fabrication (b) after N_2 annealing at 300 °C.

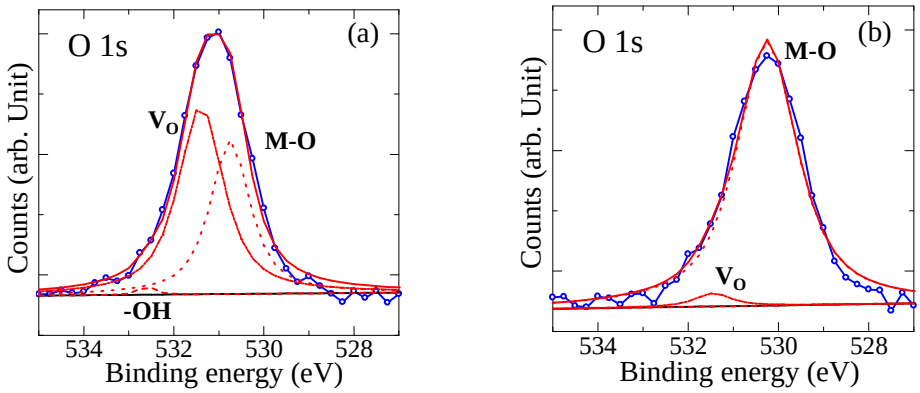


Fig. 4.3 O1s XPS spectra in IGZO films for SiN_X:F/IGZO stack films, (a) as fabrication (b) after N_2 annealing at 300 °C.

The chemical and structural evolution of a-IGZO with SiO_X and SiN_X:F films was analyzed by XPS. Figs. 4.2 and 4.3 represent the de-convolution of XPS O 1s peak measured from insulator/IGZO interface region by the method of curve fitting for as fabrication and after annealing in N_2 at 300 °C for 1h. The XPS peaks for O 1s core level demonstrate three different peaks, which can be consistently fitted by three near-Gaussians curves. The peak I, II, and III are related to OH, oxygen vacancies and meatal-oxygen (M-O) bonds. XPS result indicates that the carrier generation mechanism of both the SiO_X/IGZO and SiN_X:F/IGZO stack is shallow-donor of oxygen vacancies (Vo^+/Vo^{2+}) in as-deposited case, as shown in Fig. 4.2(a) and 4.3(a), respectively. For the SiO_X/IGZO sample, after annealing in N_2 at 300 ºC for 1h, the area ratio of Vo/M-O decreased from 1.52 to 0.57, as shown in Fig. 4.2(b), resulting in decreasing carrier concentration (Fig 6.2). Carriers in SiO_X/IGZO stack are mainly supplied from oxygen vacancies (Vo^+/Vo^{2+}). For the SiN_X:F/IGZO sample, after annealing in N_2 at 300 ºC for 1h, area ratio of Vo/M-O in SiH_X/IGZO stack drastically decreased from 1.40 to 0.03, as shown in Fig. 4.3(b). F terminated oxygen vacancies (Vo^+/Vo^{2+}) as shown in equation (4.1) [17]. Simultaneously, F can substitute for weakly bonded oxygen as shown in equation (4.2) [17]. The F 1s peak corresponding to Si-F bonds is approximately 686.3 eV at SiN_X:F bulk, while the binding energy of F 1s shifts from 686.3 to 685.5 eV which corresponds to the increase in M-F bonds, as shown in Fig. 4.4(a) and 4.4(b), respectively. F bonds more favorably with Zn than In [17], formation of Zn-F bond.

$$V_o^{\bullet\bullet} + 2e^- + F \rightarrow F_o^{\bullet} + e^- \tag{4.1}$$

$$O_o^X + F \rightarrow F_o^{\bullet} + e^- \tag{4.2}$$

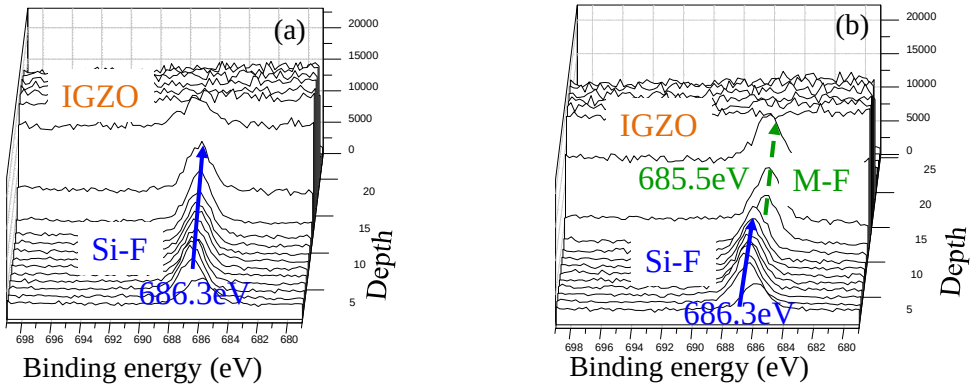


Fig. 4.4 F substitited M-O to M-F (a) as fabrication (b) after N_2 annealing at 300 °C.

It was found that F drastically reduced oxygen vacancies in IGZO after annealing. However, F substituted M-O to M-F bond and generated carriers in IGZO simultaneously. For TFT channel, F termination of oxygen vacancy is quite useful, but the number of carriers should be controlled at an appropriate level for TFT application. Therefore, the method of controlling F concentration in IGZO is essential. To control F content in an IGZO channel, we proposed a novel F doping concept. ES of SiO_X, which was formed between IGZO channel and SiN_X:F passivation layer, was used to control the F concentration in the IGZO channel. The fabrication processes of bottom-gate with ES structure oxide TFTs are described in detail in the next section.

4.2 Experimental procedure

Bottom-gate IGZO TFTs with SiO_X-ES were fabricated with SiO_X and SiN_X:F passivations, as shown in Fig. 4.5. The fabrication process for the IGZO TFTs was as follows, in which the TFTs were fabricated with an inverted staggered structure on glass substrate. First, 50 nm chromium (Cr) film was selected as gate electrode materials due to its low resistivity and smooth sidewall surface. Then, a photoresist was coated on the substrate and was exposed under a mask; finally the Cr was etched by wet-etching with HCl : H_2O_2 = 3 : 1, as shown in Fig. 4.5(a). A gate insulator of SiO_X (150 nm) was deposited at 350 °C by PE-CVD, as shown in Fig. 4.5(b). A 45-nm-thick IGZO layer was then deposited at 160 °C by direct current sputtering with a mixed gas of Ar/O_2 (29.4/0.6 sccm) at a deposition pressure of 1 Pa. An IGZO channel was defined after photolithography and dry etching with CH_4 and Ar gas mixture processes, as shown in Fig. 4.5(c). A 200-nm-thick SiO_X layer for ES was deposited at 170 °C by PE-CVD with a mixed gas of $SiH_4/N_2O/N_2$; and the ES-SiO_X was etched by dry-etching with CF_4/O_2 gas mixture, as shown in Fig. 4.5(d). Source and drain electrodes were formed by 50 nm ITO via contact holes as shown in Fig. 4.5(e). In our experiment, ITO was etched by dry-etching with CH_4 and Ar gas mixture. Following that, a 200 nm SiN_X:F layer for passivation was deposited at 200 °C on the TFT (designated “IGZO TFT with SiN_X:F-Pa”) by ICP-CVD with a mixed gas of SiF_4/N_2, as shown in Fig. 4.5 (f). Note that hydrogen-free gas chemistry was used for the SiN_X:F deposition. The F content in the SiN_X:F passivation was evaluated to be 11 at.% by Rutherford backscattering

spectrometry. An IGZO TFT with a 200-nm-thick SiO_X-Pa layer, which was deposited at 170 °C by PE-CVD with a mixed gas of $SiH_4/N_2O/N_2$, was also fabricated as a reference (designated "IGZO TFT with SiO_X-Pa"), as shown in Fig. 4.5(f). Finally, both TFTs were annealed in N_2 ambient at 350 °C for 1 and 3h. The channel length (L) and width (W) of the TFTs were 20 and 50 μm, respectively.

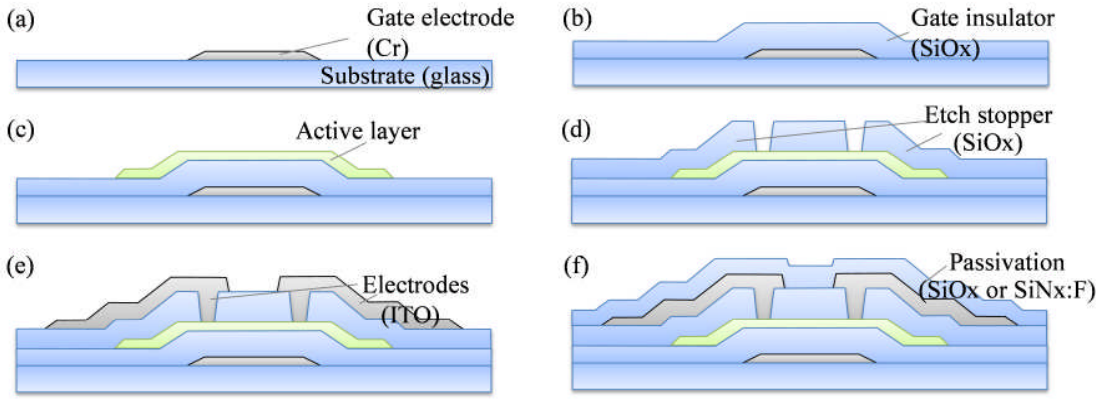


Fig. 4.5 Bottom-gate oxide TFTs fabrication processes.

All the electrical measurements were carried out in the dark and in ambient air using an Agilent 4156C precision semiconductor parameter analyzer. Under PBTS, a V_{GS} stress of +20 V was applied at stress temperatures of room temperature (RT), 50, 75, and 100 °C. In addition, source and drain electrodes were grounded, and transfer characteristics were measured at appropriate intervals with a V_{DS} of 0.1 V. During the NBIS test with a gate voltage (V_{GS}) of -20 V, a light was supplied from a Xe lamp with a band pass filter (460 nm, FWHM of 10 nm) at an intensity of 0.2 mW/cm^2. The NBIS was temporarily interrupted when the transfer characteristics measurements were performed at a V_{DS} of 0.1 V, and then NBIS was exerted again up to a stress time of 10^4 s. During photo-response measurement, light sorted by a monochromator from the output port of a Xe lamp is directed onto the sample surface through an optical fiber at an intensity of 0.2 mW/cm^2. The illumination wavelength gradually varies from 630 nm to 400 nm, as shown in Table 4.1. At each selected wavelength, the device under test is illuminated for 2min; its transfer characteristics are measured immediately without turning off the monochromatic light, and this is followed by an additional illumination/measurement

cycle. Positive constant current stability (CCS) tests were performed at a current of 120 μA at RT and 50 °C, where the drain electrode was connected to the gate electrode and the external gate bias was adjusted so as to maintain the constant current.

Table 4.1 Wavelength and photo energy corresponding table in photo-response.

Wavelength	Photo energy	Wavelength	Photo energy
dark	0.0	500 nm	2.5
630 nm	2.0	460 nm	2.7
600 nm	2.1	430 nm	2.9
560 nm	2.2	414 nm	3.0
530 nm	2.3	400 nm	3.1

4.3 Results and discussion

4.3.1 Electrical properties of IGZO TFT with SiOx or SiN_X:F passivation

Fig. 4.6 shows the transfer characteristics of the IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa after annealing at 350 °C for 1 and 3h. Threshold voltage (V_{th}) was defined by V_{GS} at a I_{DS} of 1 nA. The hysteresis of transfer curves was defined in a clockwise direction by the difference in V_{th} between forward and reverse V_{GS} sweeps. Electrical properties of the TFTs are summarized in Table 4.2.

Table 4.2 Summary of the electrical properties of IGZO TFTs.

Device name	SiO_X TFT (350°C-1h)	SiN_X:F TFT (350°C-1h)	SiO_X TFT (350°C-3h)	SiN_X:F TFT (350°C-3h)
μ ($cm^2V^{-1}s^{-1}$)	11.04	14.42	11.42	14.72
V_{th}	2.30	1.31	1.67	-0.37
Hysteresis (@V_{th} (V))	0.37	0.20	0.33	0.02
S (V/dec.)	0.28	0.25	0.29	0.19

For the TFT with SiO_X-Pa, μ, *S*, and hysteresis remained almost unchanged as the annealing time increased from 1 to 3h. However, V_{th} shifted from 2.30 to 1.67 V when the annealing time increased from 1 to 3h. On the other hand, the IGZO TFT with SiN_X:F-Pa showed a higher μ, a steeper *S*, and a smaller hysteresis than the TFT with SiO_X-Pa even after annealing for 1h. It is interesting to note that the improvements of *S* and hysteresis were confirmed for the TFT with SiN_X:F-Pa as the annealing time

increased to 3h. This result suggests that trap states existing at a GI/IGZO interface or in an IGZO are reduced by increasing the annealing time. The V_{th} of the TFT with SiN_X:F-Pa shifted from 1.31 to -0.37 V when the annealing time increased from 1 to 3h. It should be noted that the improvements of *S* and hysteresis and the increase in negative V_{th} shift through annealing for the TFT with SiN_X:F cannot be explained by the enhancement of hydrogen diffusion from SiN_X:F passivation during annealing because the SiN_X:F-Pa was deposited by the hydrogen-free gas chemistry of SiF_4/N_2. Moreover, the H content in the IGZO with SiN_X:F-Pa is expected to be similar to that of SiO_X-Pa since the H content in the IGZO is mainly affected by the deposition conditions of the SiO_X-ES layer [18]. Thus, the change in transfer characteristics suggest that F, which was introduced during the SiN_X:F-Pa deposition, passivated traps existing in the IGZO bulk and at the GI/IGZO interface during the annealing process.

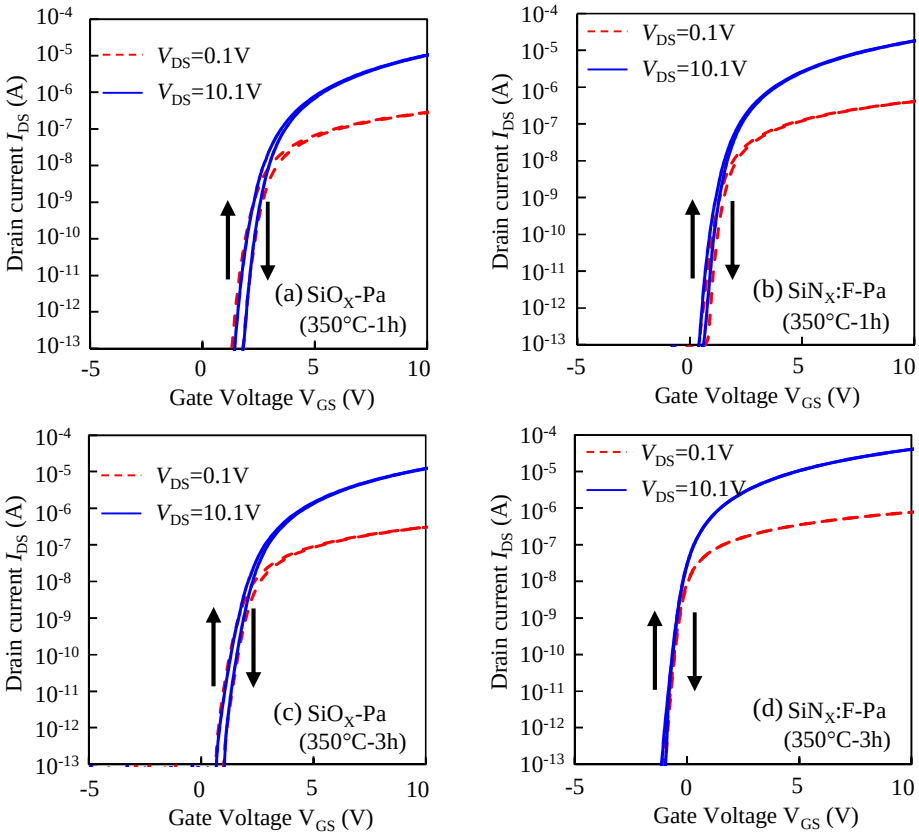


Fig. 4.6 Transfer characteristics of the TFTs with SiO_X or SiN_X:F passivation after annealing in N_2 ambient at 350 °C for different annealing times. Annealing times are (a) (b) 1h and (c) (d) 3h for the SiO_X and SiN_X:F passivations, respectively.

4.3.2 F diffusion mechanism

To determine the mechanism leading to the improved electrical properties of the TFT with SiN_X:F-Pa, the depth profiles of mass-to-charge ratios (m/z) of 1 (H) and 19 (F or OH) in the SiO_X-Pa (200 nm)/SiO_X-ES (200 nm)/IGZO (100 nm)/Si and SiN_X:F-Pa (200 nm)/SiO_X-ES (200 nm)/IGZO (100 nm)/Si stacked films were measured by SIMS using Cs^+ as a primary ion. Owing to the saturation of m/z=19 ion count in the SiN_X:F-Pa film, depth profiles of m/z=1 and 19 were recorded after the Cs^+ sputtering of the passivation layer during SIMS measurements.

Figs. 4.7(a) and 4.7(b) show depth profiles of m/z=1 and 19, respectively, in the SiO_X-ES/IGZO stack on a Si substrate with SiO_X-Pa. It is confirmed that the H (m/z=1) profile remains almost unchanged in the IGZO layer as the annealing time increases from 1 to 3h. On the other hand, although m/z=19 was detected in both of the SiO_X-ES and IGZO layers with SiO_X-Pa, as shown in Fig. 4.7(b), the detected m/z=19 is identified as that of OH ions, since fluorine was not used for the deposition of the stacked film.

Figs. 4.7(c) and 4.7(d) respectively depict m/z=1 and 19 ion profiles in the SiO_X-ES/IGZO stack with SiN_X:F-Pa. Figs. 4.7(e) and 4.7(f) respectively summarize the ion ratios of m/z=1 and 19 normalized by ^{18}O in the SiO_X-ES/IGZO stacks with SiN_X:F-Pa and SiO_X-Pa after 1h annealing. As shown in Fig. 4.7(e), no difference in H (m/z=1) content was observed in both the ES-SiO_X and IGZO between the SiN_X:F-Pa and SiO_X-Pa samples, indicating that hydrogen diffusion from the SiNx:F-Pa did not occur during the annealing. However, a large difference in m/z=19 content in the SiO_X-ES layers was observed between the SiO_X-Pa and SiN_X:F-Pa samples, as shown in Fig. 4.7(f). The large difference in m/z=19 content in the SiO_X-ES layer with SiN_X:F-Pa is attributable to fluorine, because the H profiles in the SiO_X-ES layers with SiO_X-Pa and SiN_X:F-Pa samples are almost the same. Although the result indicates that F existed in the SiO_X-ES layer with SiN_X:F-Pa, it is difficult to detect the difference in m/z=19 content in the IGZO layer between SiO_X-Pa and SiN_X:F-Pa after only 1h annealing. When the annealing time increased to 3h, an increase in m/z=19 content in the IGZO layer with SiN_X:F-Pa was detected, as shown in Fig. 4.7(h). It should be noted that the H content in the IGZO layer was no different in SiO_X-Pa and SiN_X:F-Pa even after 3h annealing, as shown in Fig. 4.7(g). These results indicate that the long annealing time enhanced F diffusion from the

SiO_X-ES layer to the IGZO channel when F existed in the SiO_X-ES layer.

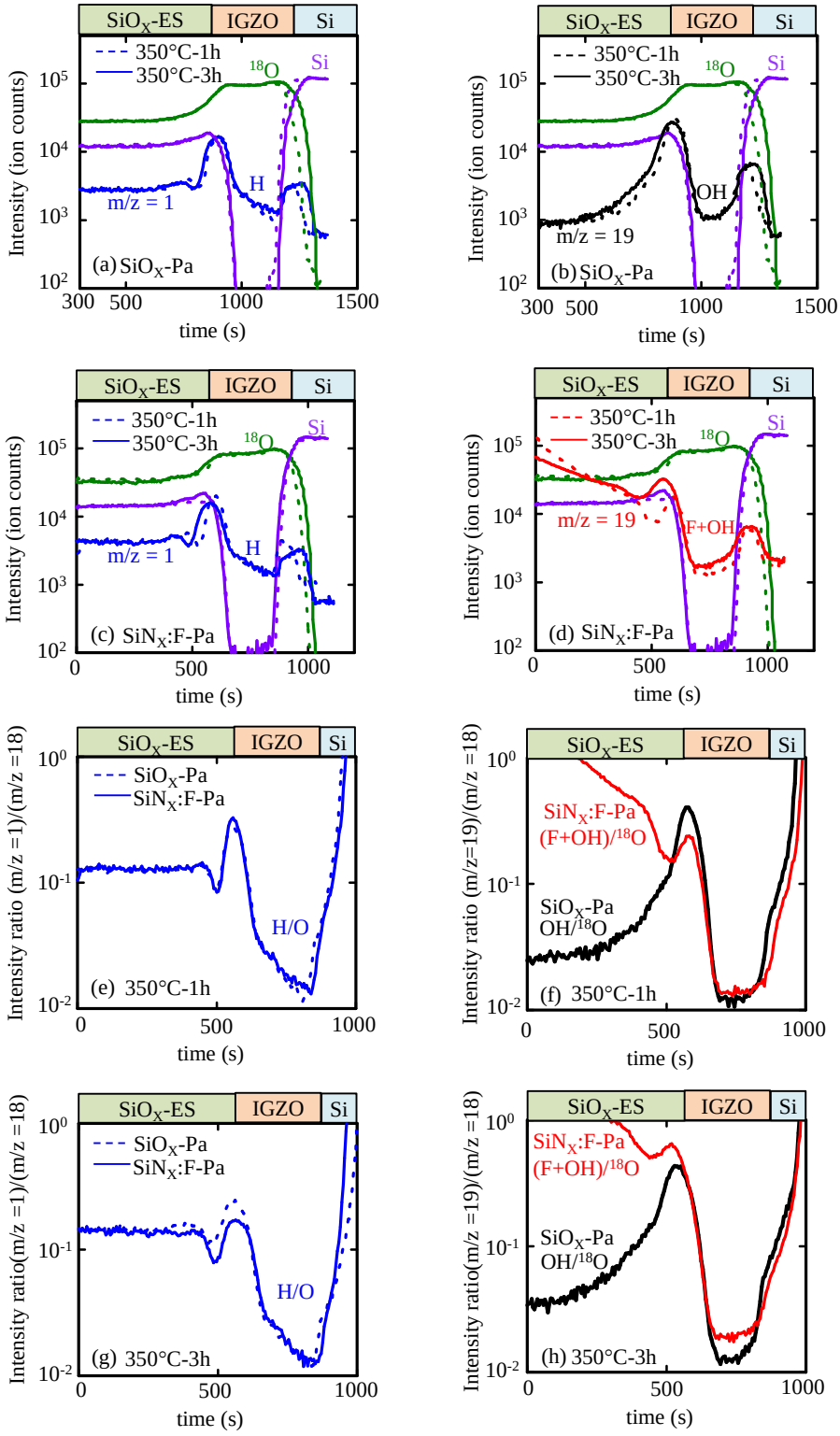


Fig. 4.7 SIMS depth profiles of (a)(c) m/z=1 (H) and (b)(d) m/z=19 in the thin-film stack

of SiO_X-ES/IGZO/Si with the SiO_X and SiN_X:F passivations after annealing at 350 °C for 1 and 3h. Normalized ion ratios of (e)(g) (m/z=1)/(m/z=18) and (f)(h) (m/z=19)/(m/z=18) in the SiO_X-ES/IGZO/Si with the SiO_X and SiN_X:F passivation after annealing at 350 °C for (e)(f) 1 and (g)(h) 3h.

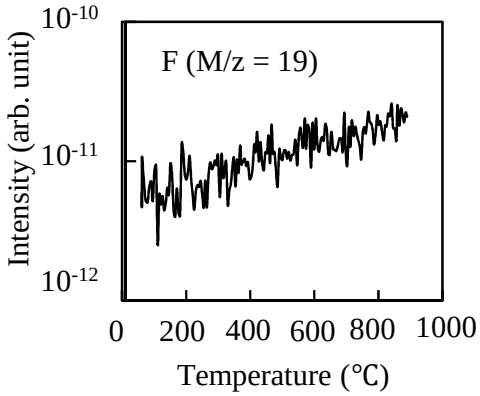


Fig. 4.8 TDS spectra of F (m/z of 19) from SiN_X:F films formed employing SiF_4/N_2.

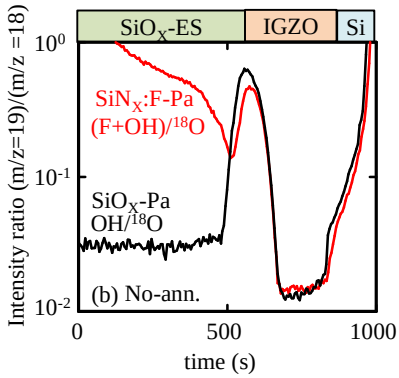


Fig. 4.9 SIMS depth profiles of (a) m/z=1 (H) and (b) m/z=19 in the thin-film stack of SiO_X-ES/IGZO/Si with the SiO_X and SiN_X:F passivations without annealing.

In order to investigate the origin of the F atom formed, a thermal desorption spectroscopy (TDS) measurement was carried out for the SiN_X:F film, as shown in Fig. 4.8. The behaviors of m/z=19 (H_3O and/or F) intensities were stable even the temperature increased to 800 °C, meaning that F^+ was not desorbed from Si-F bond in SiN_X:F film when the temperature increased. Thus, F atoms in the fluorinated SiN_X film were very stable. Then, depth profiles of m/z=19 in the SiO_X-ES/IGZO stack on a Si substrate with

SiO_X-Pa and SiN_X:F-Pa without annealing were measured, as shown in Fig. 4.9. Large differences in the m/z=19 content in the SiO_X-ES layers was observed for the SiO_X-Pa and SiN_X:F-Pa samples. The large m/z=19 content in the SiO_X-ES layer with SiN_X:F-Pa originates from fluorine. Therefore, F was introduced into the SiO_X-ES layer during the SiN_X:F-Pa deposition. SIMS results of Fig 4.7(d) also supported the mechanism. F concentration decreased at SiN_X:F-Pa/SiO_X-ES interface for 3h annealing as compared with that for 1h annealing. These results indicate that F was introduced into the SiO_X-ES layer during the SiN_X:F-Pa deposition, and did not originate from desorption of Si-F bonds.

4.3.3 Stability of IGZO TFT with SiO_X or SiN_X:F passivation

4.3.3.1 Positive gate bias and temperature stress stability

The positive gate bias and PBTS stability of IGZO TFTs is of crucial importance for their practical application; moreover, further improvement of PBTS stability is required for IGZO TFTs. It was reported that the reduction and/or passivation of traps in a channel or at a dielectric/channel interface is an effective method for improving the PBTS stability of IGZO TFTs [15]. However, the effects of F on the PBTS stability of IGZO TFTs and the mechanism for defect passivation have not been clarified in detail.

To further investigate the effect of the F passivation of traps on PBTS stability, changes in the transfer characteristics of the TFTs with SiO_X-Pa and SiN_X:F-Pa were evaluated under a V_{GS} stress of +20 V with grounded V_{DS} at stress temperatures of RT, 50, 75, and 100 °C.

Fig. 4.10 shows the PBTS results for the TFTs with SiO_X-Pa and SiN_X:F-Pa after 1h annealing. For the TFT with SiO_X-Pa, transfer curves shifted to a positive V_{GS} direction without S degradation of 3.56 V after PBTS of 10^4 s at 100 °C, as shown in Fig. 4.10(a). The stress temperature dependence of V_{th} shift, as shown in Fig. 4.10(b), indicates that the positive V_{th} shift increased with stress temperature. On the other hand, transfer curves of the TFTs with SiN_X:F-Pa shifted to a positive V_{GS} direction without S degradation of 3.08 V after PBTS of 10^4 s at 100 °C, as shown in Fig. 4.10(c). The tendency of V_{th} shift of the TFTs with SiN_X:F-Pa under stress temperature, which is shown in Fig. 4.10(d), is

very similar to that of the TFTs with SiO_X-Pa, shown in Fig. 4.10(b). The transfer curves are shifted in a positive direction by incrementing the positive gate bias stress time with no definite change in *S*. In addition, the change in mobility can be ignored with increase of the positive gate bias stress time. In previous reports, two main mechanisms for the shift in V_{th} were identified. One is electron trapping at the GI/IGZO interface [19], [20], and the other is the creation of additional defect states in the subgap states at or near the channel/dielectric interface [21], [22]. A lack of *S* variation indicates that additional defect states are not generated [23], [24]; therefore, negative charge trapping at a GI/IGZO interface and/or in a GI is the main cause of the positive V_{th} shift without *S* degradation under PBTS [25], as shown in Fig. 4.11. With increasing PBTS duration, more free electrons were trapped at the GI/IGZO interface. As a result, transfer curves shifted to a positive V_{GS} direction owing to the vertical electron field in the channel under positive V_{GS} bias.

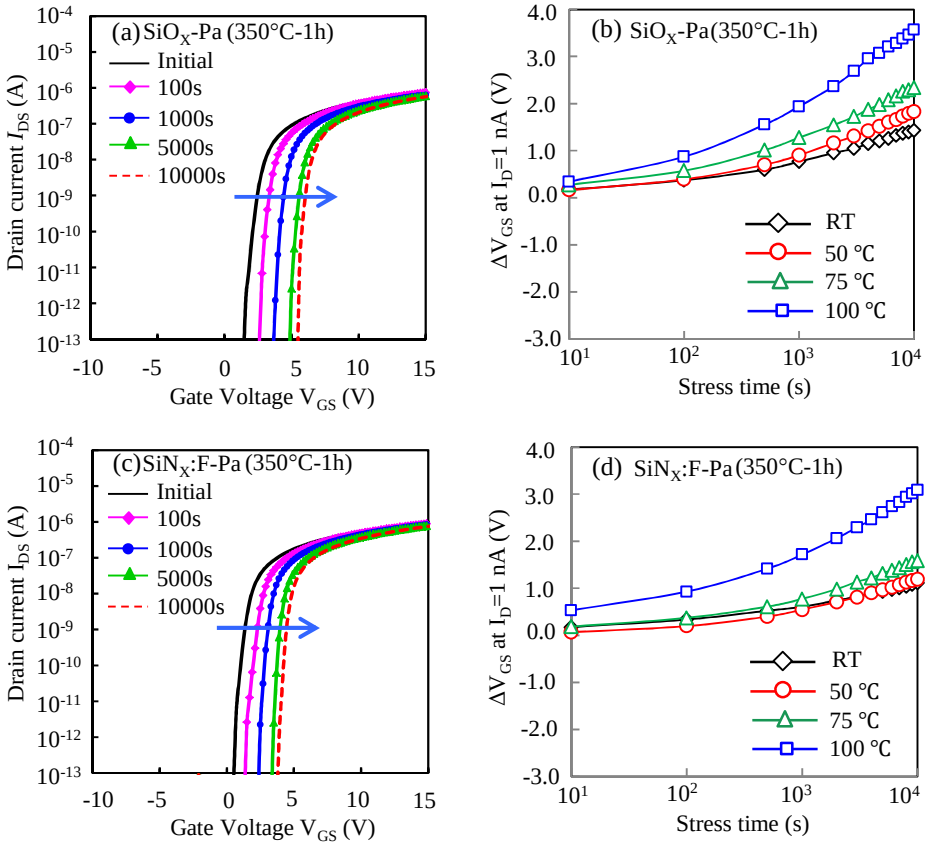


Fig. 4.10 Change in transfer characteristics during PBTS of 100 °C for the IGZO TFTs with (a) SiO_X and (c) SiN_X:F passivations after N_2 annealing at 350 °C for 1h. Threshold

voltage shift (ΔV_{th}) profiles of the TFTs with (b) SiO_X and (d) SiN_X:F passivations as a function of stress time under stress temperatures of RT, 50, 75, and 100 °C.

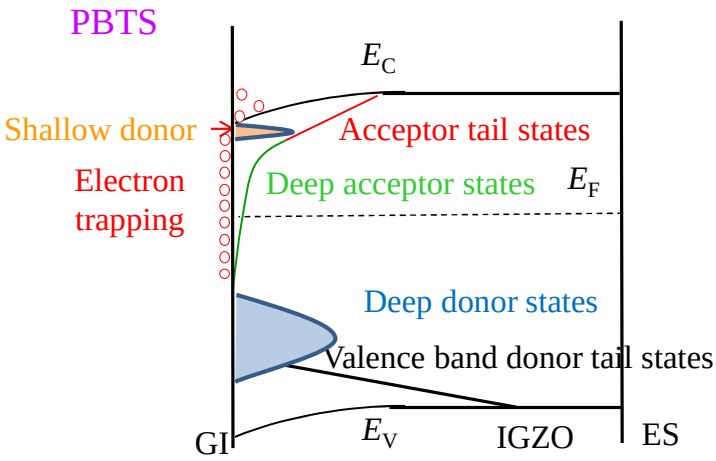


Fig. 4.11 Degradation mechanism of IGZO TFTs under PBTS after N_2 annealing at 350 °C for 1h.

When the annealing time increased to 3h, an anomalous negative V_{th} shift of -6.24 V with a hump was observed for the TFT with SiO_X-Pa under PBTS at 100 °C, as shown in Fig. 4.12(a). The negative V_{th} shift with a hump increased with increasing stress temperature for the TFT with SiO_X-Pa, as shown in Fig. 4.12(b). We reported previously that a hump was observed for a ZnO TFT owing to the creation of a donor-like state when ZnO was deposited at a low partial pressure of oxygen during ZnO sputtering [26, 27]. Therefore, the negative V_{th} shift of the TFT with a hump after 3h annealing under PBTS at 100 °C could be explained by the creation of a donor-like state in IGZO owing to the enhancement of weakly bonded Zn-O formation. A long annealing time in N_2 ambient enhances the formation of weakly bonded Zn-O in IGZO since the binding energy of Zn-O (284 kJ·mol^{-1}) is smaller than those of In-O (346 kJ·mol^{-1}) and Ga-O (374 kJ·mol^{-1}) [28], leading to the enhancement of the creation of a donor-like state under PBTS, as shown in Fig. 4.13. Note that the negative shift with S degradation increased during PBTS duration, indicating that the PBTS-induced defects must be in the bulk and existing near the Fermi level energy (E_F) at the V_{GS} of the turn-on voltage. In contrast to

the TFT with SiO_X-Pa, it should be noted that transfer curves of the TFT with SiN_X:F-Pa hardly shifted under PBTS after 3h annealing, and the V_{th} shift markedly reduced to -0.45 V after PBTS of 10^4 s even at 100 °C, as shown in Figs. 4.12(c) and 4.12(d). Hump formation and *S* degradation were completely suppressed under PBTS at 100 °C.

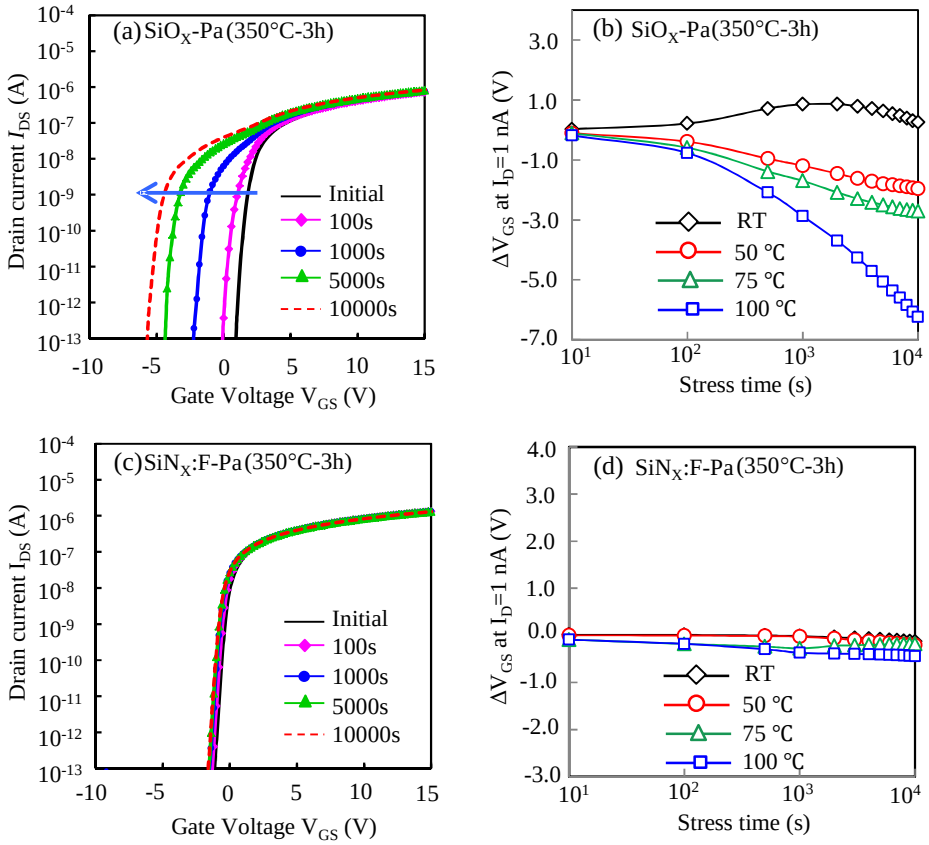


Fig. 4.12 Change in transfer characteristics during PBTS of 100 °C for the IGZO TFTs with (a) SiO_X and (c) SiN_X:F passivations after N_2 annealing at 350 °C for 3h. Threshold voltage shift (ΔV_{th}) profiles of the TFTs with (b) SiO_X and (d) SiN_X:F passivations as a function of stress time under stress temperatures of RT, 50, 75, and 100 °C.

From the SIMS analysis results mentioned previously, F diffusion into the IGZO channel was confirmed for the TFT with SiN_X:F-Pa after 3h annealing. Since fluorine and oxygen have similar ionic radii, diffused F can substitute for weakly bonded oxygen Eq. (4.2) or occupy oxygen vacancies Eq. (4.1) in the IGZO atomic structure. The substitution of an O ion with a F ion creates a free electron owing to the difference in

electrovalence between F (F^-) and O (O^{2-}) ions; thus, the carrier concentration in IGZO increased through Eq. (4.2), resulting in the negative V_{th} shift of initial transfer characteristics. On the other hand, F consumes a free electron when F passivates a doubly charged oxygen vacancy through Eq. (4.1).

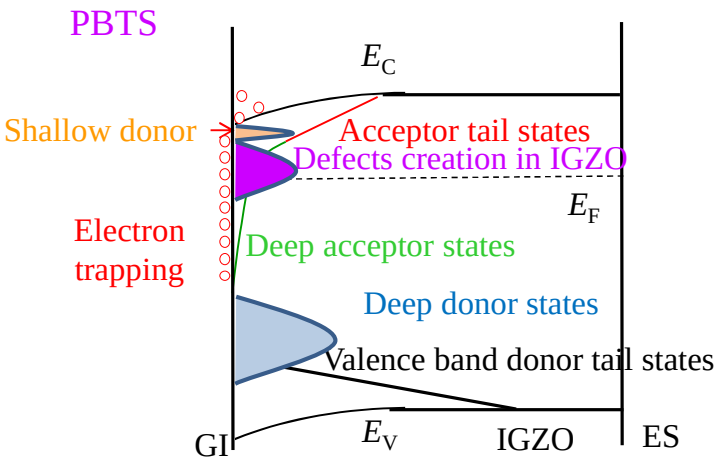


Fig. 4.13 Degradation mechanism of IGZO TFTs with SiO_X passivation under PBTS after N_2 annealing at 350 °C for 3h.

Since F bonds more favorably with Zn than with In [17], the formation of the Zn-F bond (364 kJ·mol^{-1}) [28] will play an important role in maintaining stability under thermal and electrical stresses when F substitutes O in weakly bonded Zn-O. Thus, diffused F can preferentially substitute weakly bonded oxygen: Zn-O becomes Zn-F [Eq. (4.2)]. As a consequence of the F substitution of weakly bonded ZnO to form thermally stable Zn-F, the hump could be suppressed for the TFT with SiN_X:F-Pa under PBTS at 100 °C. Moreover, since the binding energy of the Si-F (595 kJ·mol^{-1}) [28] bond is extremely high, diffused F atoms would bond with defects, such as weak Si-O bonds and oxygen vacancies, which exist at a GI/IGZO interface and/or in a SiO_X-GI [29,30], resulting in the suppression of negative charge trapping under PBTS. Hence, we can conclude that diffused F in IGZO suppressed not only the creation of a donor-like state in the IGZO bulk but also the negative charge trapping at the GI/IGZO interface and/or in the GI under PBTS, as shown in Fig. 4.14.

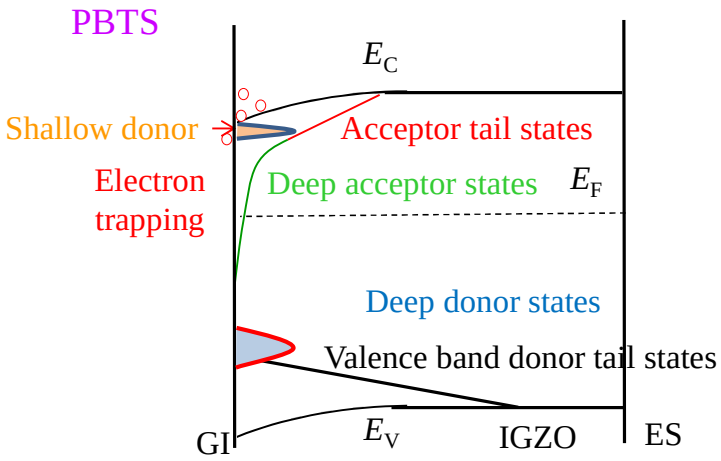


Fig. 4.14 Mechanism of IGZO TFTs with SiN_X:F passivation under PBTS after N_2 annealing at 350 °C for 3h.

SIMS analysis revealed that the PBTS stability of the IGZO TFT with SiN_X:F passivation was markedly improved when the diffusion of F into the IGZO channel from a SiO_X-ES was confirmed after post-fabrication annealing. Fluorine effectively passivated electron traps and weakly bonded oxygen in the IGZO channel and at the GI/channel interface [31]. As a consequence, for the fluorine-passivated IGZO TFT, the threshold voltage shift under PBTS with a V_{GS} stress of +20 V for 10^4 s was markedly reduced from -6.24 V for the TFT with SiO_X passivation to -0.45 V for the TFT with SiN_X:F passivation even at a stress temperature of 100 °C. A highly stable fluorine-passivated IGZO TFT was demonstrated under PBTS. The defects in the IGZO TFT were passivated by fluorine, which was introduced into a SiO_X etching stopper during the deposition of fluorinated silicon nitride for passivation and diffused during post-fabrication annealing. The fluorine-passivated IGZO TFT has improved operation temperature, and is advantageous for achieving high-performance and high-reliability oxide TFTs for next-generation displays.

4.3.3.2 Negative gate bias and illumination stress stability

Oxide TFTs have a crucial issue with regard to light stability because of their unique transparent circuit application; in particular, the NBIS is important for AMLCD [32-34]. K. Nomura et al. reported that a-IGZO contained high-density deep subgap defects with

energy level close to the valence band maximum (near VBM state) at the IGZO back-channel surface within ~2 nm [35]. The TFT degradation induced by NBIS stress is strongly affected by the density of both deep defects and electron interface traps [24]. Thus it is very important to reduce the traps to improve the NBIS stability of oxide TFT. In section 4.3.3.1, it was reported that F can effectively passivate oxygen vacancy, weakly bonded oxygen in IGZO bulk and/or at front interface. Diffused F in IGZO suppressed not only the creation of a donor-like state in the IGZO bulk but also the negative charge (electron) trapping at the GI/IGZO interface and/or in the GI. However, the effects of F passivation on deep defects and the influence of F on NBIS stability of IGZO TFTs have not been made clear.

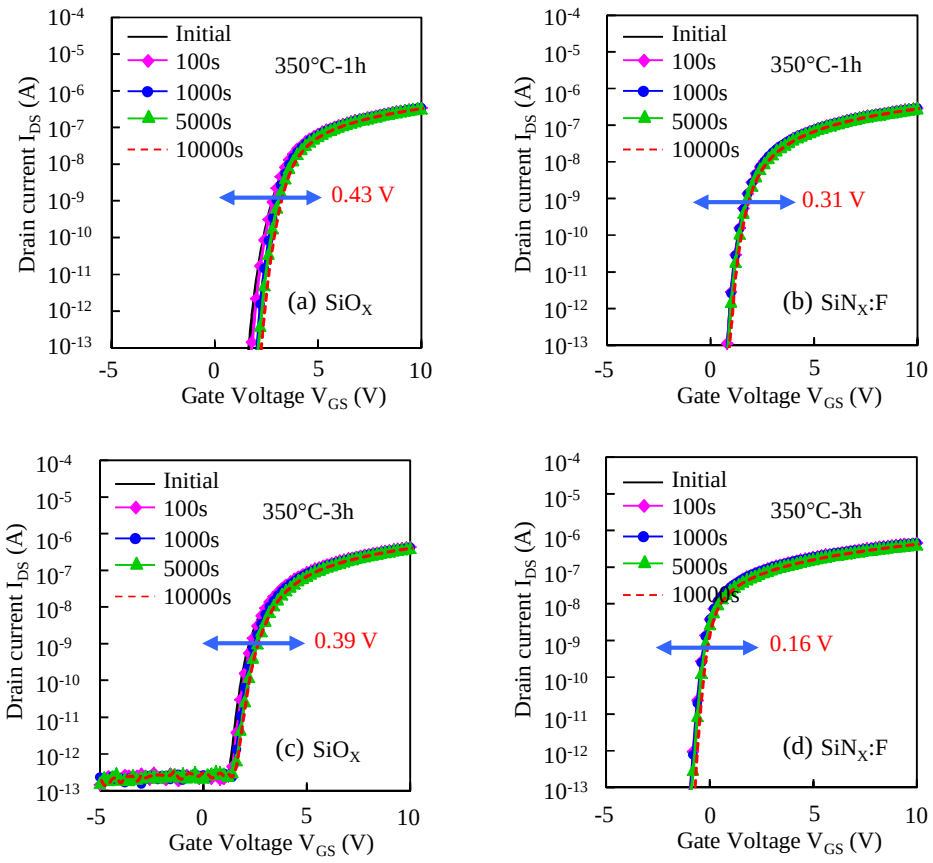


Fig. 4.15 Change in transfer characteristics during NBS without light for the IGZO TFTs with (a) SiO_X and (b) SiN_X:F passivations after N_2 annealing at 350 °C for 1h; (c) SiO_X and (d) SiN_X:F passivations after N_2 annealing at 350 °C for 3h.

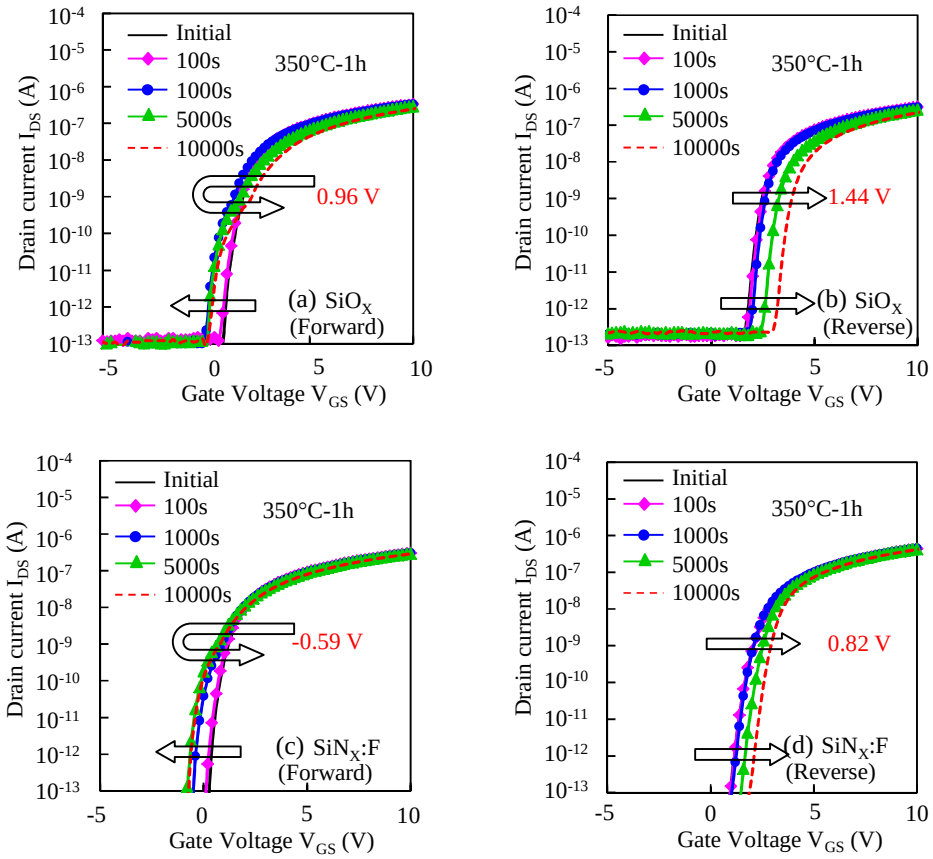


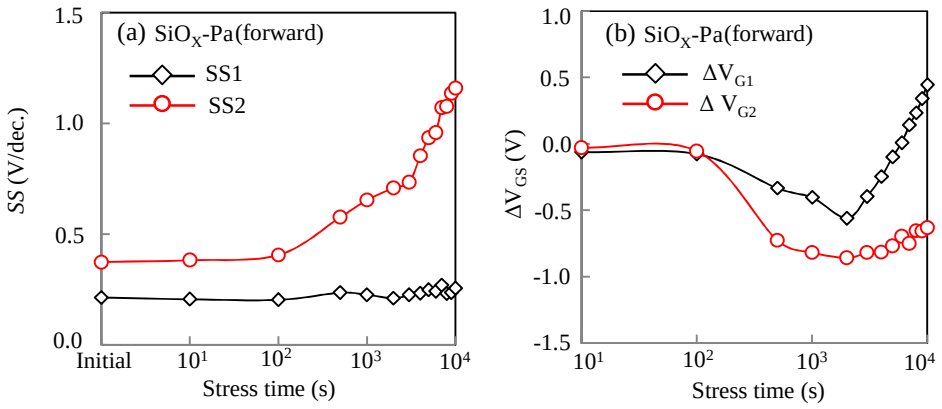
Fig 4.16 Change in transfer characteristics during NBIS (λ=460 nm) for the IGZO TFTs with SiO_X and SiN_X:F passivations after N_2 annealing at 350 °C for 1h by a double sweeping V_{GS} mode. Summarized transfer curves in (a) (c) forward and (b) (d) reverse measurements obtained from a double sweeping V_{GS} mode.

To further investigate the effect of the F passivation of deep traps on NBIS stability, changes in the transfer characteristics of the TFTs with SiO_X-Pa and SiN_X:F-Pa were evaluated under a V_{GS} stress of -20 V with grounded V_{DS} at stress temperatures of RT under blue light (wavelength of 460 nm). Photo-response was also investigated to clarify the passivation effect on NBIS stabilities of IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa.

Fig. 4.15 shows the negative bias stress (NBS) results without light illumination for the TFTs with SiO_X-Pa and SiN_X:F-Pa after 1h or 3h annealing. NBS stability of TFTs with SiO_X-Pa and SiN_X:F-Pa was very stable after 10^4 s stress after both 3h and after 1h annealing. However, when combined with light illumination, instability of V_{th} and on-

current degradation was observed after 1h annealing, as shown in Fig. 4.16(a) and 4.16(c), for IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa. To investigate the change in transfer characteristics with NBIS time, transfer characteristics were measured at various NBIS times using a double sweeping V_{GS} mode. These are respectively summarized in Figs. 4.16(a), 4.16(c) and 4.16(b), 4.16(d) for V_{GS} sweeping from -10 to 20 V (denoted hereafter as forward measurement) and from 20 to -10 V (denoted hereafter as reverse measurement). The tendency of V_{th} shift and on-current degradation of the TFTs with SiN_X:F-Pa under NBIS shown in Fig. 4.16(c) and 4.16(d) is very similar to that of the TFTs with SiO_X-Pa shown in Fig. 4.16(a) and 4.16(b). To describe the degradation phenomena clearly, several types of definition were adopted. SS1 and SS2 were respectively defined for near turn-on and threshold voltages as requiring V_{GS} from 1 to 10 pA and from 1 to 10 nA to flow I_{DS}. Moreover, V_{G1} and V_{G2} were also defined as V_{GS} at I_{DS} flowing at 1 nA and 1 pA, respectively. Figure 4.17 and 4.18 shows the changes in SS1, SS2, V_{G1}, and V_{G2} as a function of NBIS duration for IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa, respectively. In short, for those two type TFTs, SS1 was almost unchanged in the forward and reverse measurement during the NBIS duration, as shown in Fig 4.17(a), 4.17(c), 4.18(a) and 4.18(c); however, SS2 gradually degraded as the NBIS time exceeded 2000s accompanied by on-current (I_{DS} of over 0.1 nA) degradation in the forward measurement, as shown in Fig. 4.16(a), 4.16(c), 4.17(a) and 4.18(a). V_{G1} shifted towards the negative V_{GS} direction in the initial stage (<2000 s) of NBIS; however, V_{G1} shifted backwards to the positive V_{GS} direction as NBIS time further increased in the forward measurement, as shown in Fig 4.17(b) and 4.18(b). V_{G2} showed the same tendency as V_{G1} in the initial stage, and then slightly shifted to the positive V_{GS} direction as NBIS time further increased in the forward measurement, as shown in Fig 4.17(b) and 4.18(b). On-current degradation vanished; negligible changes in SS were observed in the reverse measurement, as shown in Fig. 4.16(b) and 4.16(d). In the initial stage (<2000 s) of NBIS, V_{G1} and V_{G2} slightly shifted in the positive V_{GS} direction, then, there was significantly positive shift of the transfer curve without SS degradation in the subsequent reverse measurement, as shown in Fig 4.17(d) and 4.18(d). These increases in SS2 and V_{G1} with NBIS time of over 2000s correspond to on-current degradation. To clarify the mechanism of the on-current degradation as NBIS duration exceeded 2000s, the energy-

band diagram during the stress is shown in Fig. 4.19. It has been reported elsewhere that high-density oxygen vacancies (V_O) exist in the a-IGZO bulk about 2.3 eV away from E_C [1]. In this study, photon energy of 2.7 eV was sufficient to excite neutral V_O defects to V_O^+ or V_O^{2+}, and supply free electrons to E_C. Meanwhile, the ionized V_O^+ or V_O^{2+} was simultaneously neutralized by photoexcitation from the valence band to V_O^+ or V_O^{2+}, which contributes to the generation of free holes in the valence band. NBIS-induced bistable donor-like defects originated from V_O^+ or V_O^{2+} existing near E_F, contributing to degradations of on-current and SS2. The on-current degradation was enhanced with increasing NBIS duration owing to the fact that more V_O^+ or V_O^{2+} was generated, leading to more defect creation. The donor-like defects that were generated were stabilized by capturing electrons during the forward measurement. On the other hand, these photo excited holes and electrons will be trapped at the IGZO/GI (front-channel) and the etch-stopper/IGZO (back-channel) interfaces respectively under negative V_{GS}. Since trapped holes at the front channel have a stronger influence than trapped electrons at the back-channel interface, hole trapping at the front-channel interface will be the main origin of negative transfer curve shift without SS degradation in the initial stage (<2000 s) of NBIS. With increasing NBIS duration, more free electrons were excited from neutral V_O states and drifted towards the etch-stopper/IGZO interface; furthermore, the trapped holes at the front-channel interface were detrapped immediately on applying the positive V_{GS} during the forward measurement, which resulted in significantly changes in turn-on voltage and negligible changes SS in the reverse measurement when NBIS exceed 2000s [36,37].



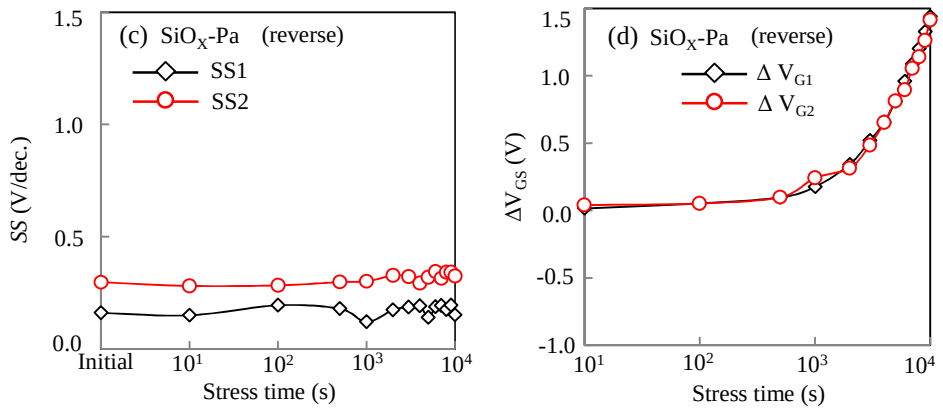


Fig. 4.17 Changes in (a) SS1 and SS2 and (b) ΔV_{G1} (I_{DS} of 1 nA) and ΔV_{G2} (I_{DS} of 1 pA) in transfer characteristics of IGZO TFTs with SiO_X:F-Pa as a function of NBIS duration of 10^4 s with grounded V_{DS}.

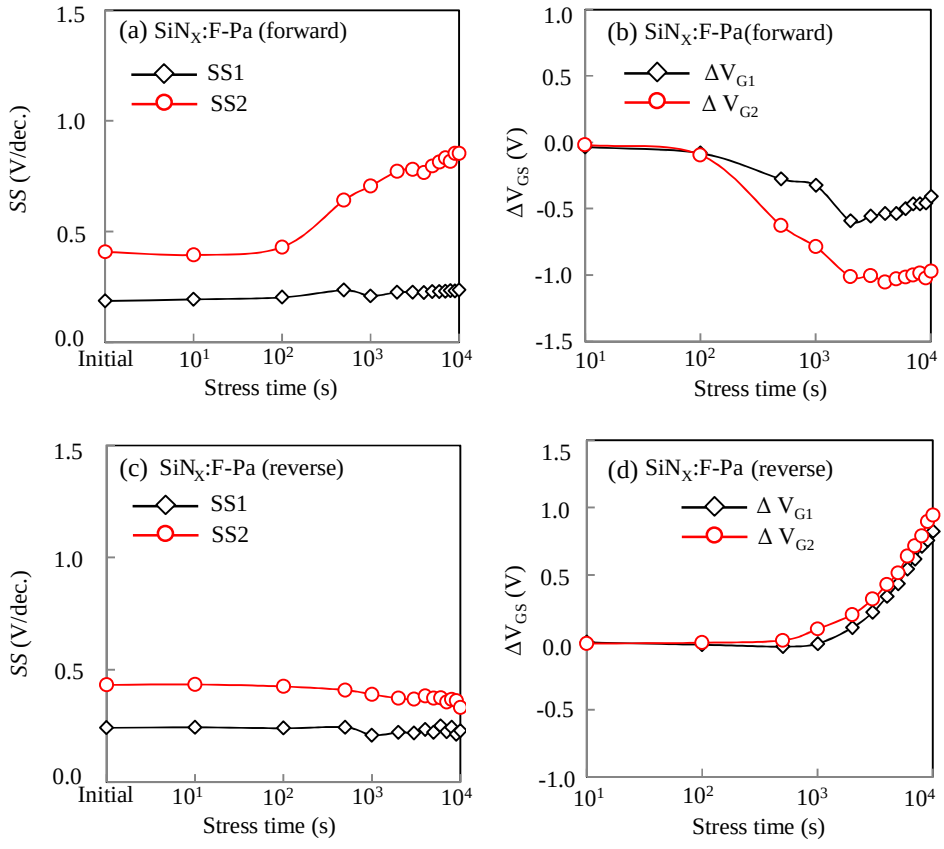


Fig. 4.18 Changes in (a) SS1 and SS2 and (b) ΔV_{G1} (I_{DS} of 1 nA) and ΔV_{G2} (I_{DS} of 1 pA) in transfer characteristics of IGZO TFTs with SiN_X:F-Pa as a function of NBIS duration of 10^4 s with grounded V_{DS}.

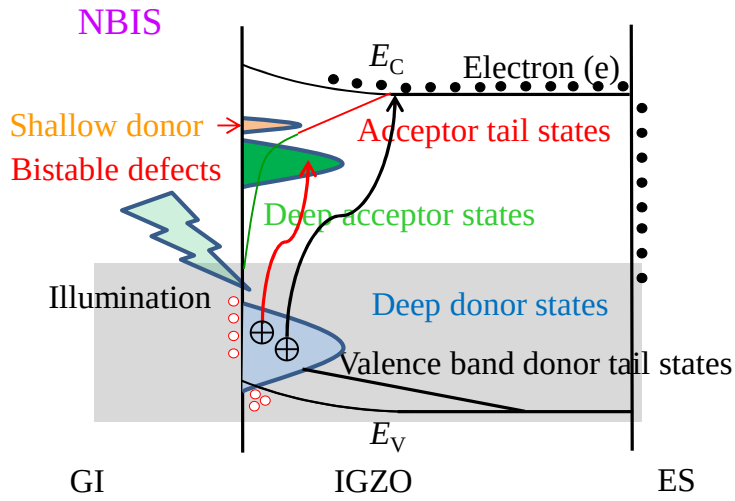


Fig. 4.19 Degradation mechanism of IGZO TFTs with SiO_X or SiN_X:F passivation under NBIS after N_2 annealing at 350 °C for 1h.

When the annealing time increased to 3h, on-current degradation in forward measurement and positive parallel shift in reverse measurement were also observed for the TFT with SiO_X-Pa under NBIS, a tendency that was similar as TFT with SiO_X-Pa after 1h annealing, as shown in Fig. 4.20(a) and 4.20(b). In contrast to the TFT with SiO_X-Pa, it should be noted that transfer curves of the TFT with SiN_X:F-Pa hardly shifted under NBIS after 3h annealing, as shown in Figs. 4.20(c) and 4.20(d). To describe the improvement phenomena clearly, the transfer characteristics of IGZO TFTs with SiO_X-Pa and SiN_X:F before and after NBIS of 10^4 s was summarized in Fig. 4.21(a) and 4.21(b). It was found that hysteresis V_H (transfer curves was defined in a clockwise direction by the difference in V_{on} between forward and reverse V_{GS} sweeps) of transfer characteristics was drastically enhanced from 0.35 V (initial) to 4.31 V by applying the NBIS of 10^4 s, as shown in Fig. 4.21(a). At the initial stage of the NBIS stress, the transfer curves shifted 1.46 V to a negative V_{GS} direction without S value degradation; subsequently, S value and on-current degradations were observed as the NBIS stress time exceeded 500 s. In contrast, for reverse measurements, the transfer curves shifted 0.97 V to a negative V_{GS} direction within 500 s, and then shifted 3.94 V to a positive V_{GS} direction without S degradation at the NBIS time of 10^4 s, as shown in Fig 4.22. NBIS degradation

mechanism of IGZO TFT with SiO_X-Pa after 3h annealing has already been described in detail for the 1h case. NBIS degradation phenomena of IGZO TFT with SiO_X-Pa were effectively suppressed by SiN_X:F passivation; forward and reverse transfer curves shifted 0.33 V and 0.19 V, respectively, even at the NBIS time of 10^4, as shown in Fig. 4.22. For IGZO TFTs with SiN_X:F-Pa, V_H shift was dramatically reduced to 0.16 V after NBIS time of 10^4 s. Hump and *S* degradation were completely absent under NBIS. NBIS-induced defects originated from V_O^+ or V_O^{2+} exciting by photons. However, for IGZO TFTs with SiN_X:F-Pa, since F has similar ionic radii to oxygen, diffused F through long time annealing can occupy oxygen vacancies and suppress the generation of V_O^+ or V_O^{2+} by photons, resulting in the improvement of NBIS stability of TFT with SiN_X:F-Pa.

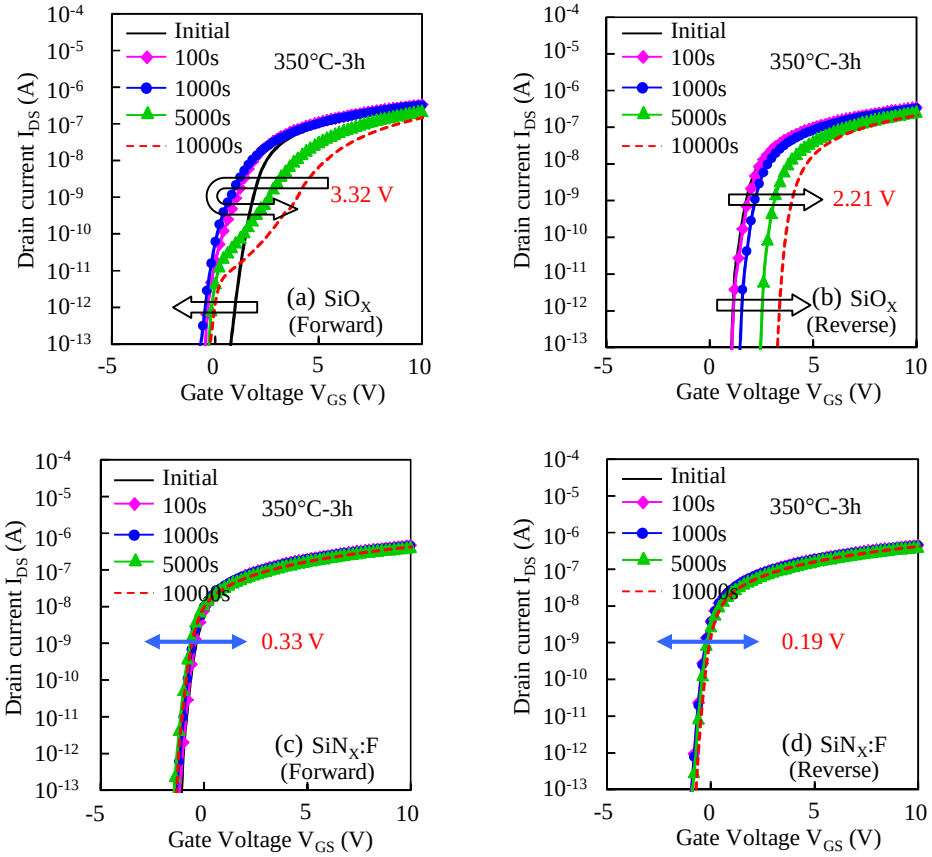


Fig. 4.20 Change in transfer characteristics during NBIS (λ=460 nm) for the IGZO TFTs with SiO_X and SiN_X:F passivations after N_2 annealing at 350 °C for 3h by a double sweeping V_{GS} mode. Summarized transfer curves in (a) (c) forward and (b) (d) reverse measurements obtained from a double sweeping V_{GS} mode.

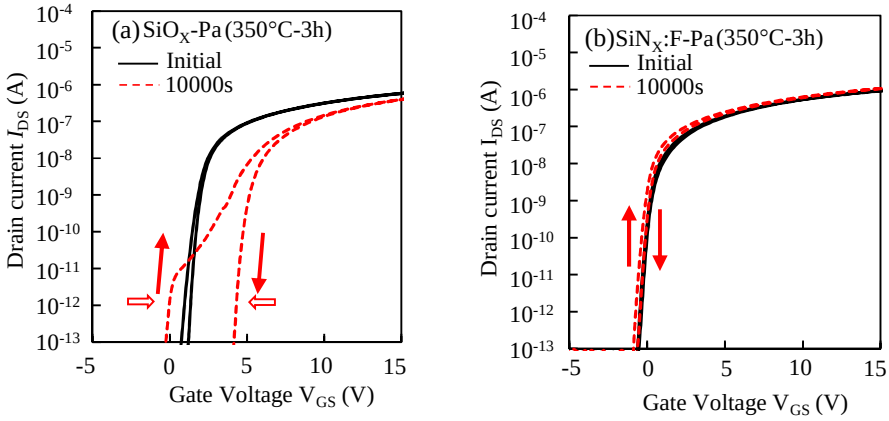


Fig. 4.21 Change in transfer characteristics during NBIS at a wavelength of 460 nm for the IGZO TFT with (a) SiO_X and (b) SiN_X:F passivation after N_2 annealing at 350 °C for 3h.

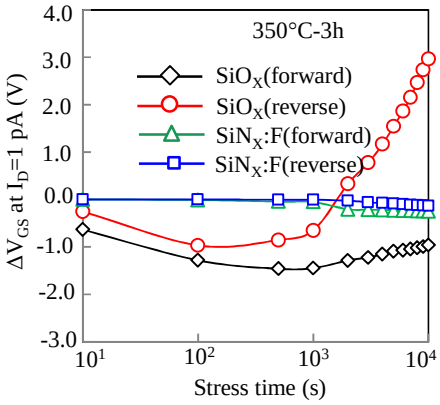


Fig. 4.22 Threshold voltage shift (ΔV_{th}) of the TFTs with SiO_X and SiN_X:F passivation as a function of NBIS stress time during forward and reverse V_{GS} sweeps.

To investigate the F passivation of deep traps, photo-response of IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa after 3h annealing was measured, as shown in Table 4.1. The mechanism of photo-response process is shown in Fig. 4.23, in which photon excited electrons were trapped by the deep traps caused by oxygen vacancy. Photo-response is an effective method to verify the change in deep traps. When a-IGZO TFT is exposed to monochromatic light, it exhibits electrical instabilities. Figs. 4.24(a) and 4.24(b) show the change of the transfer curves for the SiO_X-Pa and SiN_X:F-Pa IGZO TFTs under light illumination from the wavelengths of 500 nm to 400 nm, respectively, in logarithmic

scale. The *S* of the SiO_X TFT began to increase when the photoenergy was larger than 2.5 eV. Note that the *S* of SiN_X:F TFT increased when the wavelength was larger than 2.7 eV.

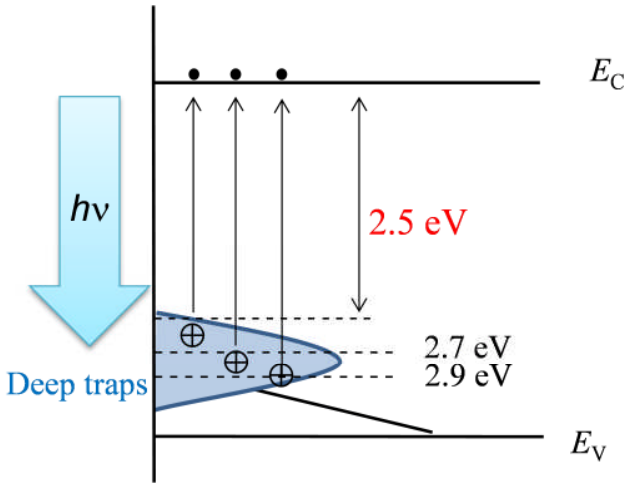


Fig 4.23 Schematic illustration of the photo-response process.

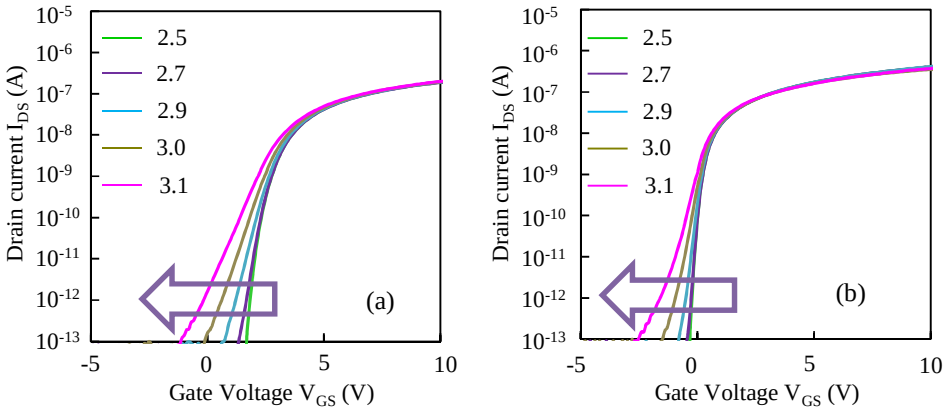


Fig. 4.24 Transfer characteristics of the stressed a-IGZO (a) SiO_X TFT, (b) SiN_X:F TFT after various monochromatic light illumination.

To clarify the origin of the passivation effect on IGZO TFT, Figs. 4.25(a) and 4.25(b) summarizes the change of *S* and V_{on} as a function of photon energy for a-IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa from the photon energy of 0 to 3.1 eV, respectively. It is obvious that ΔS and ΔV_{on} start to degrade from a photon energy of ~2.5 eV for TFT with SiO_X-Pa, while TFT with SiN_X:F-Pa remains stable under photons of higher energy up to 2.7 eV.

These results clearly show that the photo-response of the TFTs is improved by the formation of a SiN_X:F passivation layer. To clarify the mechanism of F passivation of deep traps under the NBIS duration, the energy-band diagram during the stress is shown in Fig. 4.26. Since F effectively terminated the deep defects caused by oxygen vacancies, the number of V_O^+ or V_O^{2+} was significantly decreased. Therefore, NBIS-induced bistable defects in the subgap were effectively suppressed. Photon excited holes and electrons simultaneously decreased. The effect of trapped holes at the front channel and trapped electrons at the back-channel interface was markedly reduced. So, *S* degradation was completely absent and V_H drastically improved under NBIS stress.

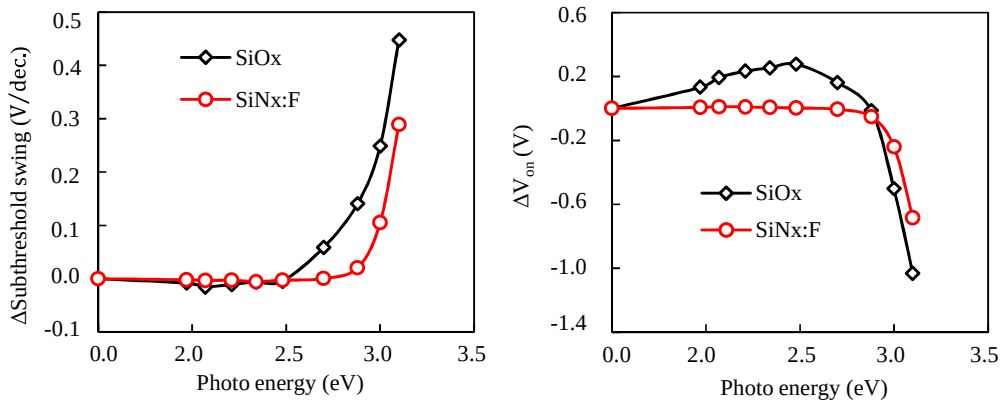


Fig. 4.25 Variation of TFT parameters (a) *S*, (b) V_{on} as a function of photon energy for a-IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa.

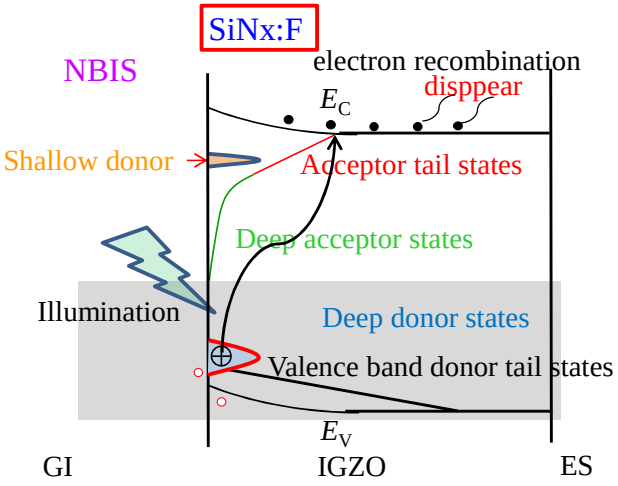


Fig. 4.26 Mechanism of IGZO TFTs with SiN_X:F passivation under NBIS after N_2 annealing at 350 °C for 3h.

We investigated the electrical properties and NBIS stability of IGZO TFTs with SiO_X and SiN_X:F passivation. Improvements in performance and NBIS stability of IGZO TFTs were achieved by SiN_X:F passivation after 3h annealing as compared with SiO_X passivation. Secondary ion mass spectrometry (SIMS) analysis revealed that NBIS stability of the IGZO TFT with SiN_X:F passivation was dramatically improved when the F diffusion into the IGZO channel through a SiO_X-etching-stopper (SiO_X-ES) was confirmed after post-fabrication annealing. Photo-response results indicate F can effectively passivate the deep defects in IGZO caused by oxygen vacancies. It was found that F can effectively passivate oxygen vacancies in IGZO or near the IGZO back-channel surface. As a consequence, for the fluorinated IGZO TFT, V_H of transfer curves under NBIS with a V_{GS} stress of -20 V for 10^4 s was drastically reduced from 4.31 V for the TFT with SiO_X passivation to 0.16 V for the TFT with SiN_X:F passivation at a wavelength of 460 nm. Fluorinated silicon nitride was used as passivation layer for fluorine source, which is compatible with large area substrates fabrication process, and without additional process and damage in the channel. The proposed method of fluorinating IGZO TFTs is therefore suitable for application in next generation FPD.

4.3.3.3 Positive bias constant current stress stability

AMOLED displays require TFTs with high current drivability to achieve uniform brightness, and the stability of the TFT under long-term current operation is critical in the case of current driven AMOLED displays because such stability influences pixel signal level/emission intensity [38-40]. Therefore, the electrical stability under turn-on state (V_{GS} and V_{DS} > 0 (CCS)) and turn-off state (V_{GS} = 0 and V_{DS} > 0) of the driving TFT is very important to the image quality of AMOLED display [41–44].

Although the data is not shown here, IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa after annealing in N_2 ambient at 350 °C for 3h under a drain bias stress (V_{GS} = 0 and V_{DS} > 0) were very stable. In this study, we mainly investigated CCS stability of IGZO TFTs with SiO_X-Pa and SiN_X:F-Pa after annealing in N_2 ambient at 350 °C for 3h. Figure 4.27 shows the variation in the transfer characteristics with CCS duration at a current of 120 μA at RT and 50 °C for the TFTs with SiO_X-Pa and SiN_X:F-Pa after 3h annealing. For the TFT with SiO_X-Pa, transfer curves shifted to a positive V_{GS} direction without *S*

degradation of 0.80 and 1.12 V after CCS of 10^4 s at RT and 50 °C, as shown in Fig. 4.27(a) and 4.27(b), respectively. The stress temperature dependence of V_{th} shift, as shown in Fig. 4.28(a), indicates that the positive V_{th} shift increased with stress temperature. On the other hand, transfer curves of the TFTs with SiN_X:F-Pa shift to a negative V_{GS} direction without S degradation of 0.07 and 0.43 V after CCS of 10^4 s at RT and 50 °C, as shown in Fig. 4.27(c) and 4.27(d), respectively. The tendency of V_{th} shift of the TFTs with SiN_X:F-Pa under stress temperature shown in Fig. 4.28(b), indicates that the negative V_{th} shift increases with stress temperature. CCS stabilities of TFTs with SiO_X-Pa and SiN_X:F-Pa are both very stable after 10^4 s stress after 3h annealing, moreover, TFTs with SiN_X:F-Pa is a little better.

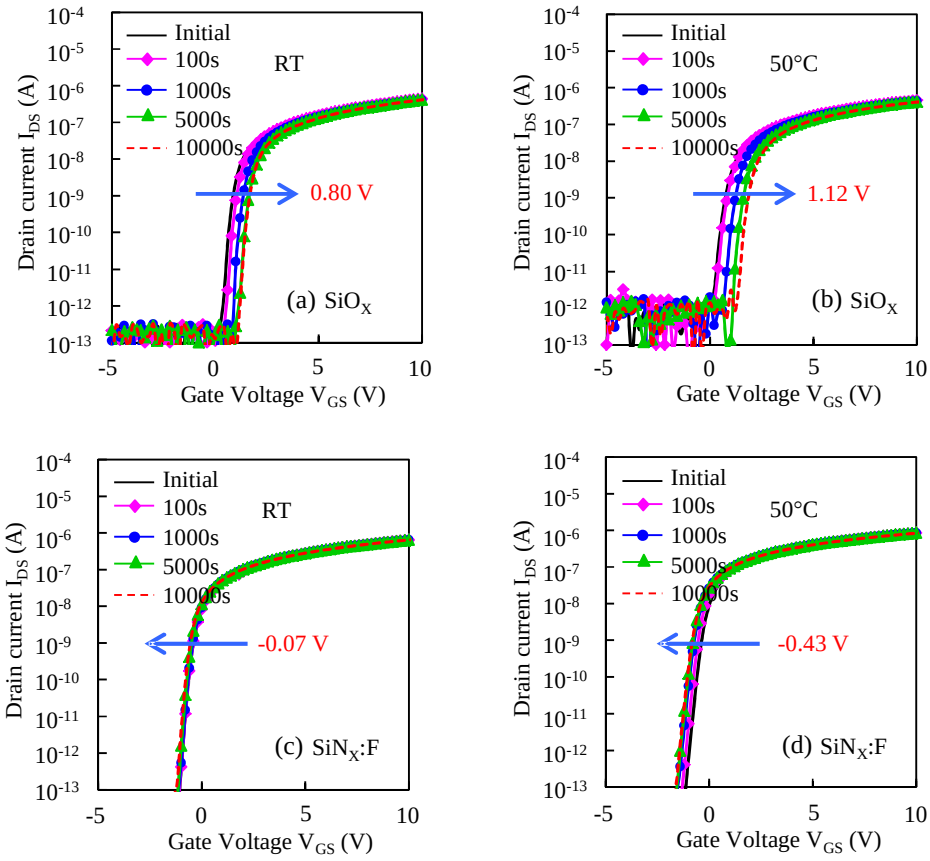


Fig. 4.27 Change in transfer characteristics during CCS for the IGZO TFTs with SiO_X and SiN_X:F passivations after N_2 annealing at 350 °C for 3h at (a) (c) RT, (b) (d) 50 °C.

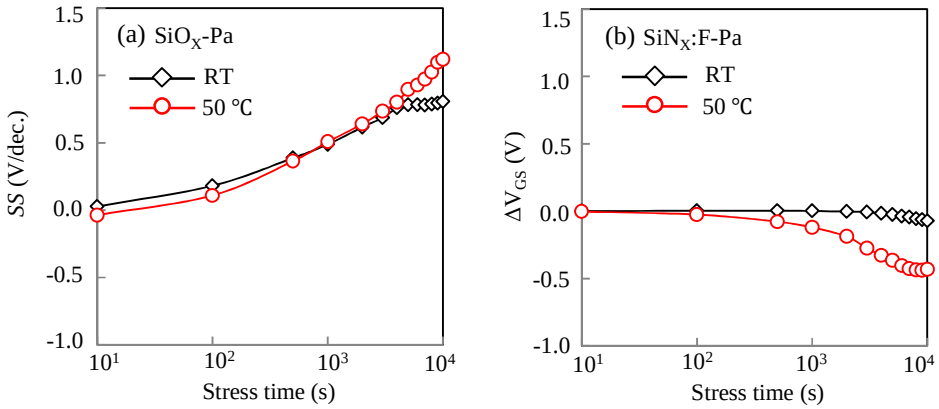


Fig. 4.28 Threshold voltage shift (ΔV_{th}) profiles during CCS of the TFTs with (b) SiO_X and (d) SiN_X:F passivations as a function of stress time under stress temperatures of RT, 50 °C.

4.4. Conclusions

We tried to achieve high performance and highly stable oxide TFTs using SiN_X:F as a fluorine source. To control F content in an IGZO channel, we proposed a novel F doping concept. Etch-stopper of SiO_X, which was introduced between IGZO channel and SiN_X:F passivation layer, was used to control the F concentration in the IGZO channel.

The electrical properties and bias stress stabilities of IGZO TFTs with SiN_X:F or SiO_X passivation were investigated. Improvements in the performance and stabilities of IGZO TFTs were achieved by SiN_X:F passivation as compared with SiO_X passivation through long time annealing. For the fluorine-passivated IGZO TFT, the ΔV_{th} under PBTS with a V_{GS} stress of +20 V for 10^4 s was markedly reduced from -6.24 V for the TFT with SiO_X passivation to -0.45 V for the TFT with SiN_X:F passivation, even at a stress temperature of 100 °C. We investigated the NBIS stability of a-IGZO TFT by using a double sweeping V_{GS} mode of transfer characteristics measurement. V_H of transfer curves under NBIS with V_{GS} stress of -20 V for 10^4 s was drastically reduced from 4.31 V for the TFT with SiO_X passivation to 0.16 V for the TFT with SiN_X:F passivation at a wavelength of 460 nm. Furthermore, the fluorine-passivated IGZO TFTs also had high stability under CCS which is an important factor for AMOLED.

SIMS analysis revealed that the stabilities of IGZO TFT with SiN_X:F passivation was markedly improved when the diffusion of F into the IGZO channel from a SiO_X etching stopper (SiO_X-ES) was confirmed after post-fabrication annealing. We found that diffused F effectively passivated oxygen vacancies and weakly bonded oxygen in the IGZO channel and at the GI/channel interface, resulting in improving performance and stabilities of IGZO TFTs including PBTS, NBIS and CCS stabilities. The proposed method of fluorinating IGZO TFTs is therefore suitable for application in next generation FPD.

4.5 References

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Chapter 5
Highly stable F+ passivated IGZO TFTs

5.1 Introduction

Chapter 4 introduced highly stable fluorine-passivated IGZO TFTs. The initial performance and stabilities of the IGZO TFT with SiN_X:F passivation was markedly improved when the diffusion of F into the IGZO channel from a SiO_X etching stopper (SiO_X-ES) was confirmed using SIMS analysis after 3h post-fabrication annealing in N_2 ambient at 350 °C [1]. Based on the results reported in chapter 4, fabrication parameters of F concentration in SiN_X:F passivation were further optimized to reduce the post-fabrication annealing time.

In this study, the electrical properties and stabilities of IGZO-TFT with high F concentration (SiN_X:F+) passivation were investigated. After post annealing at 350 °C in N_2 ambient for 1h, the IGZO TFTs with SiN_X:F+ passivation showed steep *S*, low V_{th}, small hysteresis V_H; highly stable stabilities under PBTS, NBIS and CCS stress and good uniformity. The electrical properties and stabilities of IGZO TFTs with SiN_X:F+ passivation after 1h annealing was comparable to that of IGZO TFTs with SiN_X:F passivation after 3h annealing. We successfully achieved high performance fluorine-passivated IGZO TFTs by increasing the F concentration in SiN_X:F passivation layer and thus reducing the annealing time. SIMS results revealed that 1h annealing is enough for F diffusion from the SiO_X-ES layer to the IGZO channel, if larger F existed in the SiO_X-ES layer. The highly stable F+ passivated IGZO TFT has good stabilities and uniformity, and is advantageous for achieving high-performance and high-reliability oxide TFTs for next-generation displays.

5.2 Experimental procedure

Bottom-gate IGZO TFTs with SiO_X-ES were fabricated with SiN_X:F+ passivation, the detail fabrication processes of which were described in chapter 4 [2]. F content in the SiN_X:F passivation was evaluated to be 11 atom% by Rutherford backscattering spectrometry. F content in the SiN_X:F+ passivation was increased to about 20 atom% in order to increase the F concentration in ES-SiO_X layer. All the electrical measurements

were carried out in ambient air using an Agilent 4156C precision semiconductor parameter analyzer with or without light.

5.3 results and discussions

5.3.1 Electrical properties of IGZO TFTs with SiN_X:F+ passivation

Transfer characteristics (I_{DS}-V_{GS}) of IGZO TFTs with SiN_X:F+ passivation after 1h annealing were measured at a V_{DS} of 0.1 V and 10.1 V, as shown in Fig. 5.1. The IGZO TFT with SiN_X:F+ passivation showed steep subthrehold swing (<0.20) and small hysteresis (<0.10), which is comparable with that of IGZO TFTs with SiN_X:F passivation after 3h annealing. In addition, V_{th} of IGZO TFT with SiN_X:F+ passivation shifted to positive V_{GS} of about 1 V as compared with IGZO TFTs with SiN_X:F passivation after 3h annealing. The electrical properties are summarized in Table 5.1.

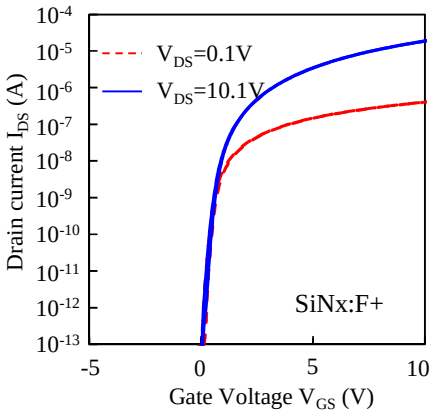

Fig. 5.1 Transfer characteristics of the TFTs with SiN_X:F+ passivation after annealing in N_2 ambient at 350 °C for 1h.

Table 5.1 Summary of the electrical properties of IGZO TFTs with SiN_X:F+ passivation.

Device name	SiN_X:F+ TFT (350°C-1h)
μ ($cm^2V^{-1}s^{-1}$)	14.52
V_{th}	0.66
Hysteresis (@V_{th} (V))	0.09
S (V/dec.)	0.16

5.3.2 Stabilities and uniformity of IGZO TFTs

Fig. 5.2 shows the PBTS results for the TFTs with SiN_X:F+-Pa after 1h annealing. Changes in the transfer characteristics of the TFTs with SiN_X:F+-Pa were evaluated under a V_{GS} stress of +20 V with grounded V_{DS} at stress temperatures of RT, 50, 75, and 100 °C. For the TFT with SiN_X:F+-Pa, transfer curves shifted to a positive V_{GS} direction without S degradation of 0.28 V after PBTS of 10^4 s at RT, as shown in Fig. 5.2(a). The stress temperature dependence of V_{th} shift, as shown in Fig. 5.2(b). The positive V_{th} shift increased with stress temperature. Finally, transfer curves of the TFTs with SiN_X:F+-Pa shifted to a positive V_{GS} direction of 0.87 V with no definite change in S after PBTS of 10^4 s at 100 °C. A lack of S variation indicates that the free electrons were trapped at the GI/IGZO interface owing to the fact that vertical electron field in the channel under positive V_{GS} bias induced the positive V_{th} shift.

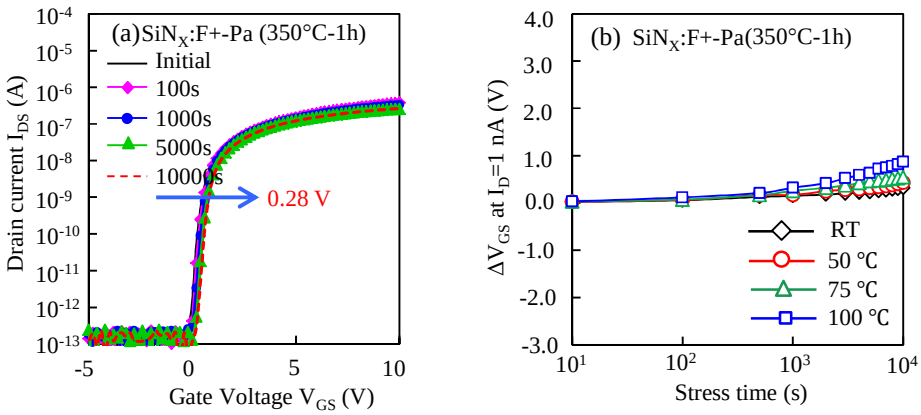

Fig. 5.2 (a) Change in transfer characteristics during PBTS at RT for the IGZO TFTs with SiN_X:F+ passivations after N_2 annealing at 350 °C for 1h. (b) Threshold voltage shift (ΔV_{th}) profiles of the TFTs with SiN_X:F+ passivations as a function of stress time under stress temperatures of RT, 50, 75, and 100 °C.

Changes in the transfer characteristics of the TFTs with SiN_X:F+-Pa were evaluated under a V_{GS} stress of -20 V with grounded V_{DS} at stress temperatures of RT with or without blue light (wavelength of 460 nm).

Fig. 5.3 shows the NBS results without light illumination for the TFTs with SiN_X:F+-

Pa after 1h annealing. Transfer curves shifted only 0.27 V during NBS of 10^4 s at RT; NBS stability of TFTs with SiN_X:F+-Pa was quite stable after 10^4 s stress after 1h annealing. Subsequently, when we combined with light illumination, the transfer curves of the TFT with SiN_X:F+-Pa also hardly shifted under NBIS after 1h annealing, as shown in Figs. 5.4(a) and 5.4(b). NBIS degradation phenomena of IGZO TFT with SiO_X-Pa were also effectively suppressed by SiN_X:F+ passivation; forward and reverse transfer curves shifted 0.28 V and 0.28 V even at the NBIS time of 10^4 s, respectively. For IGZO TFTs with SiN_X:F+-Pa, V_H shift was dramatically reduced to 0.12 V after NBIS time of 10^4 s.

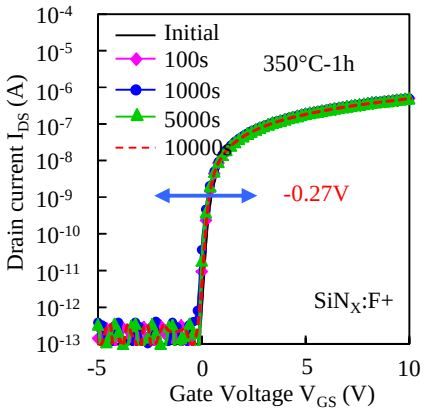

Fig. 5.3 Change in transfer characteristics during NBS without light for the IGZO TFTs with SiN_X:F+ passivations after N_2 annealing at 350 °C for 1h.

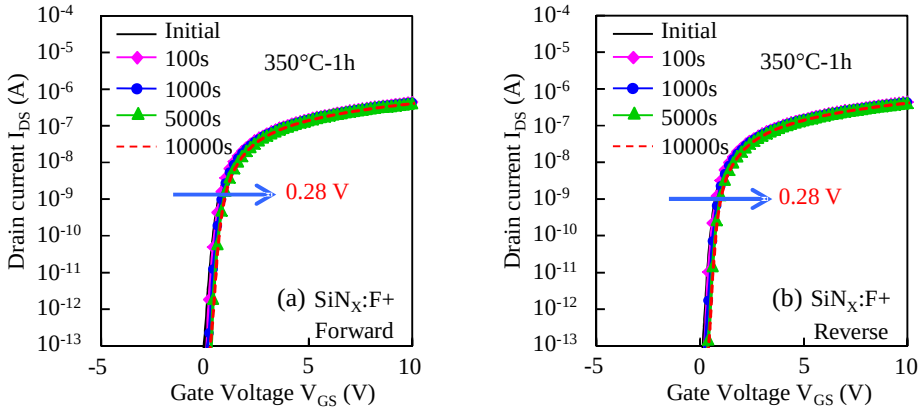

Fig. 5.4 Change in transfer characteristics during NBIS (λ=460 nm) for the IGZO TFTs

with SiN_X:F+ passivations after N_2 annealing at 350 °C for 1h by a double sweeping V_{GS} mode. Summarized transfer curves in (a) forward and (b) reverse measurements obtained from a double sweeping V_{GS} mode.

CCS stability of IGZO TFTs with SiN_X:F+-Pa after annealing in N_2 ambient at 350 °C for 1h was also investigated. Figure 5.5 shows the variation in the transfer characteristics with CCS duration at a current of 120 μA at RT and 50 °C for the TFTs with SiN_X:F+-Pa after 1h annealing. For the TFT with SiN_X:F+-Pa, transfer curves shifted to a negative V_{GS} direction of 0.12 and 0.5 V after CCS of 10^4 s at RT and 50 °C, as shown in Figs. 5.5(a) and 5.5(b), respectively. CCS stability of IGZO TFTs with SiN_X:F+-Pa was also very stable.

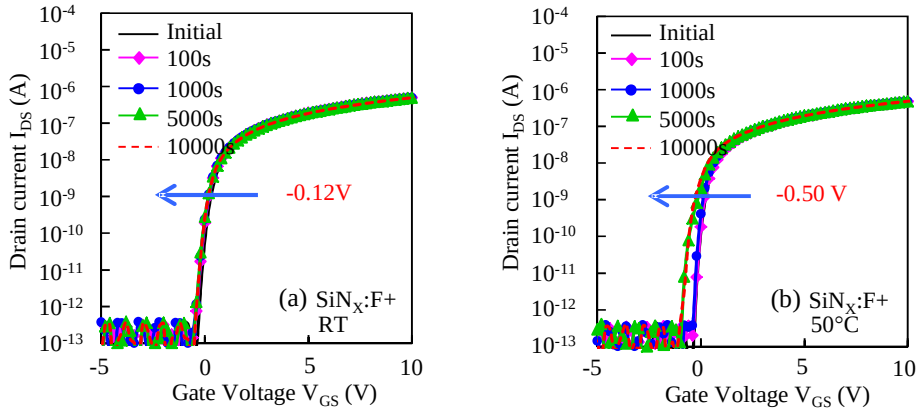

Fig. 5.5 Change in transfer characteristics during CCS for the IGZO TFTs with SiN_X:F+ passivations after N_2 annealing at 350 °C for 1h at (a) RT, (b) 50 °C.

The stabilities of the IGZO TFT with SiN_X:F+-Pa after 1h annealing under PBTS, NBIS and CCS were also investigated. High stabilities under PBTS, NBIS and CCS stress of IGZO TFTs were achieved using SiN_X:F+ passivation layer. The electrical property and stabilities of IGZO TFTs with SiN_X:F+ passivation after 1h annealing was comparable to that of IGZO TFTs with SiN_X:F passivation after 3h annealing. Subsequently, we compared the uniformity between SiN_X:F+-pa TFTs after 1h annealing and SiN_X:F-pa TFTs after 3h annealing. Fig. 5.6 shows the transfer characteristics of

these fifteen TFTs with (a) SiN_X:F+-pa TFTs after 1h annealing and (b) SiN_X:F-pa TFTs after 3h annealing. The transfer characteristics were measured at V_{DS} of 10.1 V in a single sweep V_{GS} mode (off-to-on). The uniformity of the TFTs with SiN_X:F+-pa after 1h annealing drastically improved as compared with that of SiN_X:F-pa TFTs after 3h annealing. Especially, the variation in the V_{th} was reduced from -0.30 ± 0.39 V for SiN_X:F-pa TFTs after 3h annealing to 0.64 ± 0.13 V SiN_X:F+-pa TFTs after 1h annealing, as shown in Fig. 5.7(a). The variation in the V_H was reduced from 0.22 ± 0.19 V SiN_X:F-pa TFTs after 3h annealing to 0.08 ± 0.04 V for SiN_X:F+-pa TFTs after 1h annealing, as shown in Fig. 5.7(b). The improvements in uniformity of SiN_X:F+-pa TFTs can possibly be attributed to the lower number of traps within the channel or at the channel/dielectric interfaces. The mechanism that results in improvements in uniformity of SiN_X:F+-pa TFTs still needs further investigation.

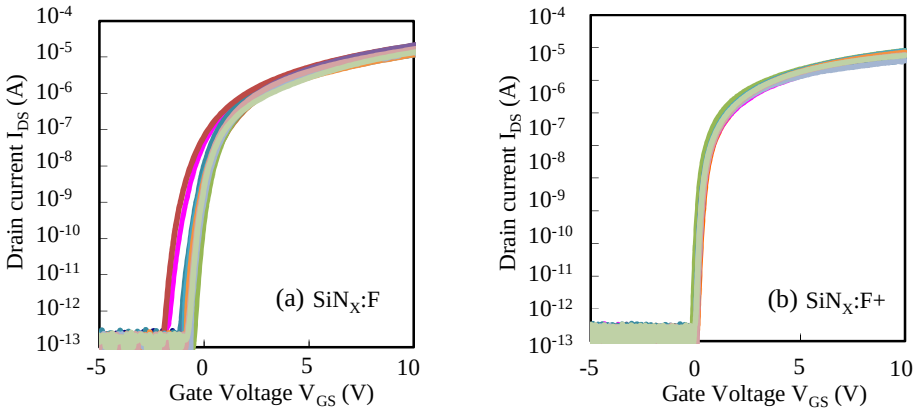

Fig. 5.6 Variation in the transfer characteristics of fifteen TFTs (a) SiN_X:F (b) SiN_X:F+ within an area of 1500 μm × 2500 μm. Transfer characteristics were measured with a V_{DS} of 10.1 V.

5.3.3 Mechanism of reducing annealing time

To clarify the origin of the reduction of annealing time for TFTs with SiN_X:F+-Pa as compared with SiN_X:F-Pa, depth profile of m/z= 19 in the SiO_X-ES/IGZO was measured. Figs. 5.8 summarize the depth profile in the SiO_X-ES/IGZO with SiN_X:F+-Pa and SiN_X:F-Pa without annealing. A large difference of m/z=19 content in the SiO_X-ES layers was observed between the SiN_X:F+-Pa and SiN_X:F-Pa TFTs. It is confirmed that the F

(m/z=19) profile larger for SiN_X:F+-Pa TFTs as compared with SiN_X:F-Pa TFTs. This result indicated that larger F content introduced to SiO_X-ES layer during the deposition of SiN_X:F+-Pa can effectively reduce the annealing time.

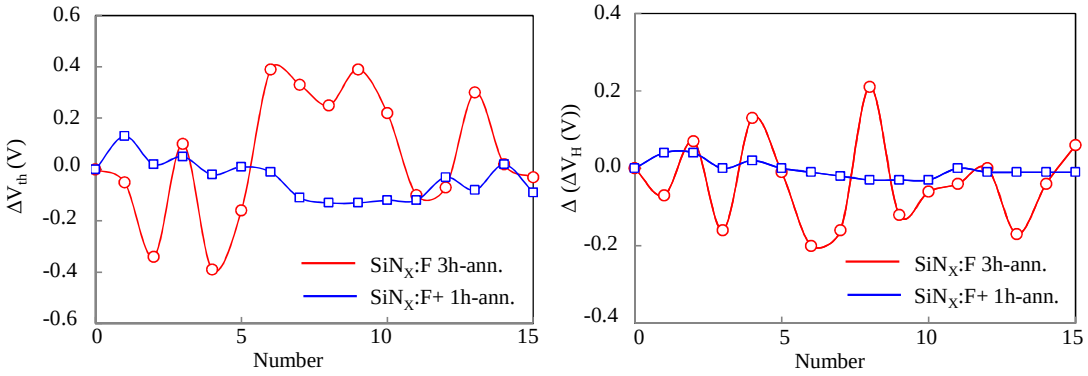

Fig. 5.7 Comparison the uniformity of (a) V_{th} and (b) ΔV_H in the transfer characteristics of fifteen TFTs between SiN_X:F-Pa and SiN_X:F+-Pa TFTs.

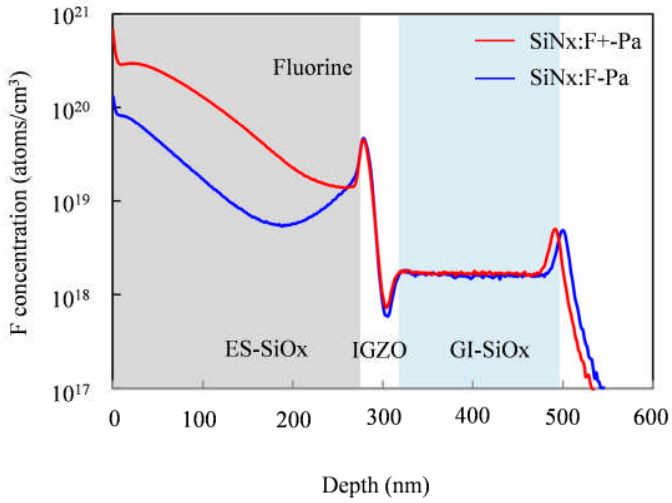

Fig. 5.8 SIMS depth profiles of m/z=19 in SiO_X-ES/IGZO with the SiN_X:F+ and SiN_X:F passivation without annealing.

5.4 Conclusions

Advanced optimization of fabrication parameters of F concentration in SiN_X:F passivation were further discussed. The electrical property and stability of IGZO-TFT

with SiN_X:F+ passivation were investigated. After post annealing at 350 °C in N_2 ambient for 1h, the IGZO TFTs with SiN_X:F+ passivation showed steep *S*, low V_{th}, small hysteresis, high stability under PBTS, NBIS and CCS stress and good uniformity - comparable to that of IGZO TFTs with SiN_X:F passivation after 3h annealing. We successfully achieved high performance fluorine-passivated IGZO TFTs by increasing the F concentration in SiN_X:F passivation layer and thus reducing the annealing time. SIMS results revealed that 1hour annealing is sufficient for F diffusion from the SiO_X-ES layer to the IGZO channel, if larger F exists in the SiO_X-ES layer. The highly stable F+ passivated IGZO TFT has good stabilities and uniformity, and is therefore advantageous for application in next-generation displays.

5.5 Reference

[1] J. Jiang, M. Furuta, and D. Wang, “Self-aligned bottom-gate In-Ga-Zn-O thin-film transistor with source/drain regions formed by direct deposition of fluorinated silicon nitride,” IEEE Elec. Dev. Lett. Vol. 35, No. 9, pp. 933-935, (2014).

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Chapter 6

Self-aligned bottom-gate IGZO TFT with source/drain regions formed by direct deposition of fluorinated silicon nitride

6.1 Introduction

Recently, TFTs based on zinc oxide and its variants, such as IGZO, are being pursued as replacements of the silicon-based TFTs for FPD and other applications [1-3]. A bottom-gate with an etch-stopper structure has been widely employed for oxide TFTs. However, one serious drawback of this structure is the large parasitic capacitance of gate-to-drain (C_{GD}) and gate-to-source (C_{GS}), owing to the overlap between gate and source/drain (S/D) electrodes. It is known that the parasitic capacitance reduces the operating speed of the TFT circuits, and induces signal delay in the TFT backplane. Moreover, for an organic light-emitting diode display, large C_{GD} of selecting TFT in a pixel strongly influences the uniformity of luminescence of pixels. This is because the C_{GD} is the main cause of kickback/feedthrough voltage, which influences the operating voltage of the driving TFT in a pixel. Therefore, a self-aligned structure is an essential requirement for oxide TFTs in order to achieve system-on-panel and high-resolution LCD and OLED displays.

There are several reports on IGZO homo-junction with highly conductive IGZO regions, which were formed by the selective exposure of Ar, H_2, or He plasma [4,5] or ion implantation of dopant [6,7]. However, it was reported that the performance of IGZO TFTs with S/D regions doped by H_2 or Ar plasma treatment can easily degrade after thermal annealing around 200-250 °C [5,6,8]. On the other hand, the IGZO homojunction was also demonstrated by the Al reaction method [8], or hydrogen diffusion from hydrogenated SiNx (SiNx:H) deposited on top of the IGZO [9-11]. A self-aligned double-gate IGZO TFT has been demonstrated on flexible substrate by using back-side exposure technique [12].

In this chapter, we proposed a novel method for making thermally stable IGZO homojunction with highly conductive region that is selectively formed by a direct deposition of SiN_X:F on top of the IGZO film. By combining the back-side-exposure technique and IGZO homojunction formed by the direct deposition of SiN_X:F on the

IGZO, a bottom-gate and self-aligned (BGSA) IGZO TFT is developed.

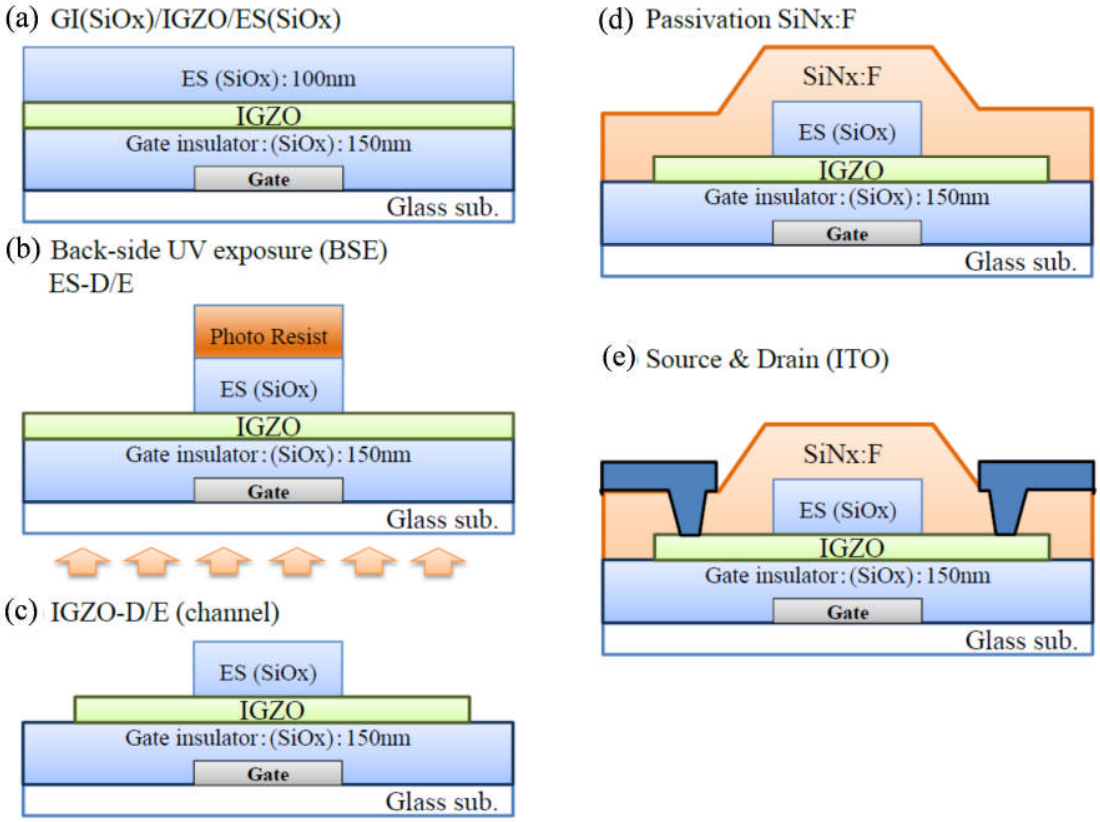

Fig. 6.1 Fabrication process steps of self-align bottom-gate IGZO TFT.

6.2 Experimental procedure

Fig. 6.1 shows the steps in the fabrication process for the developed self-aligned bottom-gate IGZO TFT. First, Cr gate electrode was formed on a glass substrate. Next, a 150-nm thick SiO_X for gate insulator was deposited at 350 °C by PECVD. A 45-nm-thick IGZO for active channel was deposited at 160 °C by DC magnetron sputtering; then, a 100-nm-thick SiO_X for ES was deposited on the IGZO by PE-CVD, as shown in Fig. 6.1(a). Following that, a photoresist was coated on the substrate and exposed from backside of the substrate (back-side exposure) using gate electrode as a mask, and the ES-SiO_X was etched by dry-etching with CF_4/O_2 gas mixture, as shown in Fig. 6.1(b). After definition of the IGZO channel as an active channel, as shown in Fig. 6.1(c), SiN_X:F for passivation was deposited by ICP-CVD using SiF_4/N_2 gas mixture, as shown in Fig. 6.1(d). Note that hydrogen-free gas chemistry was used for the SiN_X:F deposition.

Finally, source and drain electrodes were formed by indium-tin-oxide (ITO) via contact holes, as shown in Fig. 6.1(e). An IGZO TFT with a SiO_X passivation deposited at 170 °C by conventional PECVD, using a $SiH_4/N_2O/N_2$ gas mixture, was also fabricated for comparison. Deposition rate of the SiO_X and SiN_X:F passivation is 8 and 15 nm/min, respectively. Note that there is no overlap between gate and S/D electrodes. TFT properties were measured by Agilent 4156C semiconductor parameter analyzer in dark and ambient air after post-fabrication annealing at 300 °C for 1h in N_2. In addition, Hall device with Van der Pauw geometry was integrated into the TFT substrate to measure the resistivity of the IGZO in S/D regions ($\rho_{S/D}$). Thus, measured $\rho_{S/D}$ value has the same processing history as the S/D region of the TFT. Due to the limitations of Hall measurement, high resistive samples with $\rho_{S/D}$ of over 10 Ωcm in Fig. 6.3(a) were measured by two-terminal resistor, which was also integrated into TFT substrate, with the width and length of 50 and 20 μm, respectively.

6.3 Results and discussion

6.3.1 Resistivity and thermal stability of IGZO/SiO_X and IGZO/SiN_X:F stacks

To investigate the $\rho_{S/D}$ and thermal stability of IGZO/SiO_X and IGZO/SiN_X:F stacks for application in the S/D region of the TFT, the annealing temperature dependence of the $\rho_{S/D}$ was evaluated, as shown in Fig. 6.2(a). For the IGZO/SiO_X stack, $\rho_{S/D}$ was 1.9×10^{-2} Ωcm before annealing (same as just after TFT fabrication). The low $\rho_{S/D}$ of as-fabricated IGZO/SiO_X stack may have originated from plasma damage during SiO_X deposition and dry-etching. However, recovery of the $\rho_{S/D}$ was observed after N_2 annealing at 250 °C, and the $\rho_{S/D}$ increased further to over $2\times10^{+8}$ Ωcm as the annealing temperature increased to 300 °C.

On the other hand, $\rho_{S/D}$ of as-fabricated IGZO/SiN_X:F stack was 3.3×10^{-3} Ωcm, which was approximately one order of magnitude lower than that with SiO_X passivation. It was reported that fluorine acts as a shallow donor in ZnO [13] and IGZO [14]. Since fluorine and oxygen have a similar ionic radius, fluorine can be substituted for oxygen, or can occupy oxygen vacancy in an IGZO. The substitution of an oxygen ion with a fluorine ion generates free electrons, owing to the difference in electrovalency between oxygen

(O^{2-}) and fluorine (F^-) ions [15]. Hence, $\rho_{S/D}$ of the as-fabricated IGZO/SiN_X:F stack was lower than that of the IGZO/SiO_X stack. In contrast to the annealing temperature dependence of the $\rho_{S/D}$ of IGZO/SiO_X stack, the $\rho_{S/D}$ of IGZO/SiN_X stack was quite stable after annealing, and it was maintained at 4.1×10^{-3} Ωcm even after N_2 annealing at 350 °C. Carrier concentration in IGZO/SiN_X:F stack was estimated by Hall measurement, and at the annealing temperatures of 200~400 °C it was very stable in the range of $9.6\sim8.6\times10^{19}$ cm^{-3}. Thus, thermally stable $\rho_{S/D}$ could be achieved by direct deposition of SiN_X:F on top of the IGZO. These results indicate that the low $\rho_{S/D}$ of the IGZO/SiN_X:F stack and its thermal stability are very suitable for application in the S/D regions of the IGZO TFTs. It has also been reported that fluorine bonds more favorably with zinc than indium, and that a Zn-F bond is more stable than a Zn-O bond [15]. Thus, thermally stable $\rho_{S/D}$ could be achieved by a direct deposition of SiN_X:F on top of the IGZO.

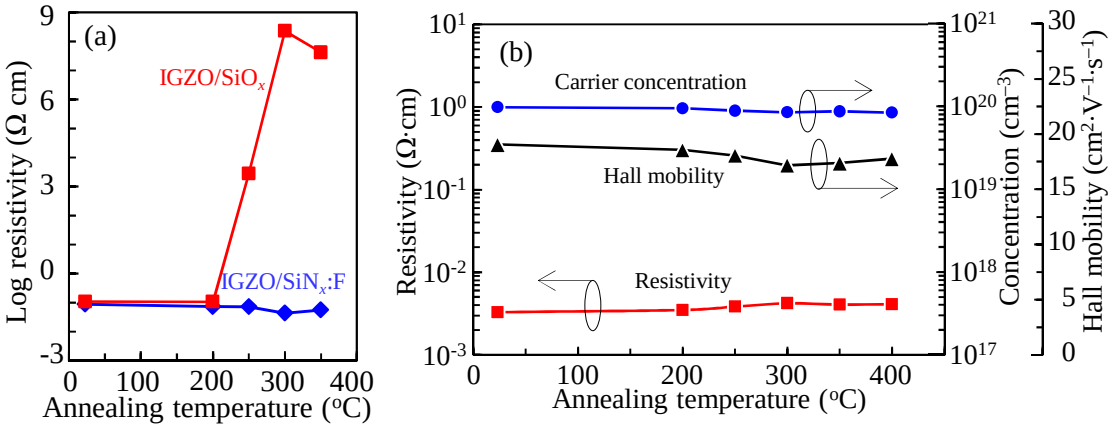

Fig. 6.2 (a) Resistivity of IGZO/SiO_X and IGZO:SiN_X:F stacks, and (b) carrier concentration and Hall mobility of IGZO/SiNx stack as a function of annealing temperature.

6.3.2 Electrical properties of self-aligned bottom-gate IGZO TFT

To investigate the effects of $\rho_{S/D}$ on electrical properties of IGZO TFT, two types of the SABG TFT with S/D regions formed by IGZO/SiO_X or IGZO/SiN_X:F stack were fabricated.

Fig. 6.3 shows the output and transfer characteristics of the IGZO TFT (W/L=66/12 μm) with (a), (b) SiO_X and (c), (d) SiN_X:F passivation, which were measured after

annealing at 300 °C. As shown in Fig. 6.3(a) and (b), the IGZO TFT with SiO_X passivation exhibited very low drain current - below 0.1 nA - even at V_{GS} of 20 V and V_{DS} of 10.1 V, which is due to the huge series resistance of the S/D regions. As mentioned in Fig. 6.2(a), $\rho_{S/D}$ of the IGZO/SiO_X stack rapidly increased when the annealing temperature exceeded 250 °C. Since the TFT characteristics were measured after post fabrication annealing of 300 °C, the high $\rho_{S/D}$ of the S/D region created serious parasitic resistance between channel and S/D region due to the presence of the offset region between channel and S/D contacts. These parasitic and offset resistances suppressed drain current, especially at low-V_{DS} region, which is confirmed by the output characteristics shown in Fig. 6.3(a). The results of the TFT with IGZO/SiO_X also indicates that the ES dry-etching with CF_4/O_2 plasma, which was shown in Fig. 6.1(c), did not contribute to forming S/D regions in the TFT after annealing.

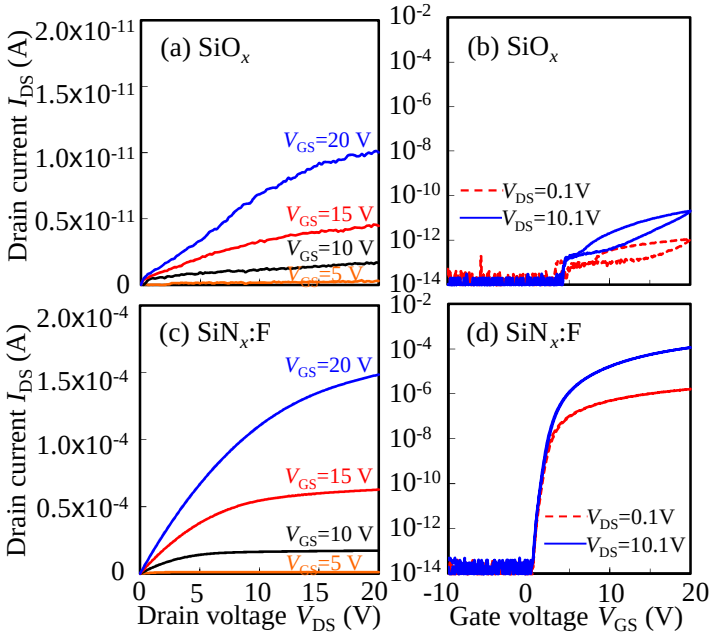

Fig. 6.3 Output and transfer characteristics of IGZO TFTs (W/L=66/12 μm) with (a)(b) SiO_X and (c)(d)SiN_X:F passivation after N_2 annealing at 300 °C.

In contrast, the TFT with SiN_X:F passivation, which is shown in Fig. 6.3(c) and (d), exhibited a drastic improvement in the drain current with the μ of 10.6 $cm^2V^{-1}s^{-1}$. Current crowding was not observed in the low-drain voltage regions of output characteristics,

indicating negligible influence of the series resistance of S/D regions ($R_{S/D}$), including offset resistance between gate and S/D contacts. This result indicates that low-resistive and thermally stable IGZO/SiN_X:F stack is an essential requirement for application in S/D regions of BGSA IGZO TFTs. As a consequence of its thermally stable $\rho_{S/D}$, the TFT with SiN_X:F passivation exhibited good electrical properties with negligible series resistance in the S/D regions after annealing at 300 °C. Moreover, the S/D regions of TFT with SiN_X:F passivation can also be applied as a connecting layer in a pixel circuit in an OLED display, because the sheet resistance of $R_{S/D}$ (840 Ω/□) is lower than 10 kΩ/□ [9].

6.3.3 Fluorine diffusion and its influence on effective channel length of the TFTs

In this section, we will discuss fluorine diffusion from SiN_X:F films into IGZO channel during post-fabrication annealing, and its influence on effective channel length (L_{eff}) of the TFT because the side-diffusion of fluorine reduce the L_{eff}. The L_{eff} was evaluated using total channel resistance (R_{tot}) as a function of physical channel length (L_P), measured by a scanning electron microscope (SEM). Fig. 6.4(a) and 6.4(b) show R_{tot} of the TFTs measured at V_{DS} of 0.1 V (V_{DS}<<V_{GS}) as a function of L_P after post-fabrication annealing at 300 and 350 °C, respectively.

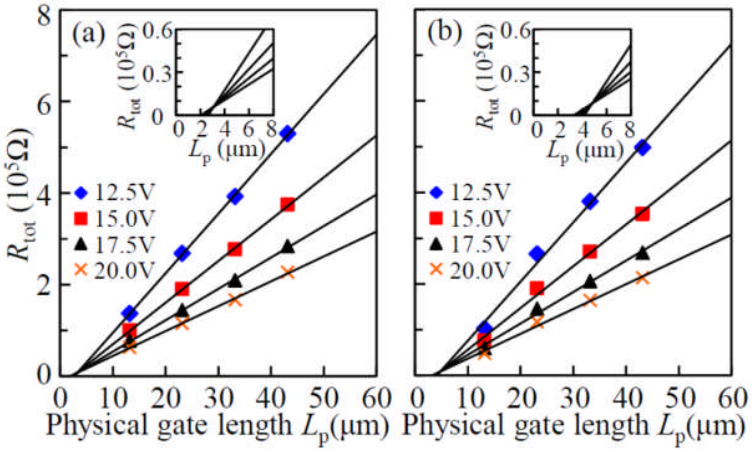

Fig. 6.4 Total resistance (R_{tot}) of the TFT (W=66 μm) with IGZO/SiN_X:F stacked S/D regions after annealing at 300 °C as a function of physical gate length (L_P). The inset shows a magnified view in the small R_{tot} region.

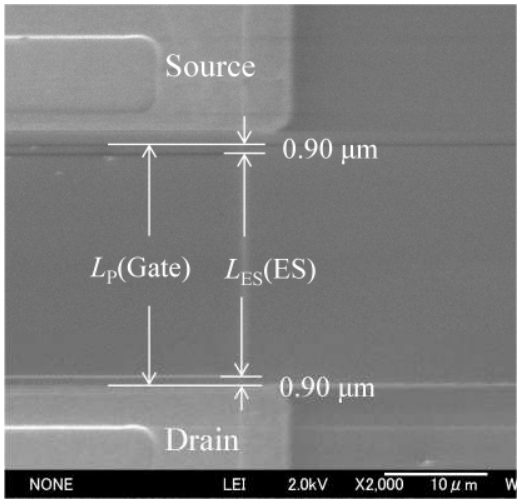

Fig. 6.5 SEM images of self-align bottom-gate IGZO TFT.

Under the (V_{GS}-V_{th})≫V_{DS}/2 condition, R_{tot} can be expressed as

$$R_{tot} = \frac{L_p - \Delta L}{W \mu_{eff} C_{ox} (V_{GS} - V_{th})} + R_{S/D} \quad (6.1)$$

where W is the channel width, μ_{eff} is the effective mobility, C_{ox} is the gate insulator capacitance/unit area, V_{th} is the threshold voltage, $R_{S/D}/2=R_S=R_D$, and ΔL is defined as L_P-L_{eff}. Since equation (6.1) gives $R_{tot}=R_{S/D}$ at $L_P=\Delta L$, a plot of R_{tot} versus L_P for the TFTs with different L_P in Fig. 6.4(a) has lines at V_{GS} of 12.5-20 V and V_{DS} of 0.1 V intersecting at one point, giving both $R_{S/D}$ and ΔL. From Fig. 6.4(a), $R_{S/D}$ and ΔL were evaluated to be 5.5 kΩ and 3.1 μm, respectively. Thus, the width-normalized $R_{S/D}$ ($R_{S/D}$W) of 33 Ωcm was obtained. To ascertain the reason for the decreasing L_{eff} (ΔL), the difference between the ES length and L_P (ΔL_{ES}) was measured by SEM, as shown in Fig. 6.5. The real ΔL can be defined as (L_P-ΔL_{ES})-L_{eff} in bottom-gate TFT. The ΔL_{ES} was measured to be 1.8 μm by SEM, which can be attributed to the over-dose of the back-side exposure process and critical dimension loss during the ES dry-etching. Thus, real ΔL, which may have originated by fluorine side-diffusion, was estimated to be 1.3 μm (0.65 μm for each side) after N_2 annealing at 300 °C. In the same manner, it was found that the ΔL_D increased from 1.3 to 3.0 μm when the post-fabrication annealing temperature increased from 300 to 350 °C, as shown in Fig. 6.4(b). This result provides evidence that the fluorine in SiN_X:F diffused into IGZO channel and contributed to form S/D regions by the IGZO/SiN_X:F stack. Although the atomic radius of fluorine is larger than that of

hydrogen, the obtained fluorine side diffusion length is comparable or longer when compared with hydrogen diffusion length reported in Refs. 9 and 16. We confirmed that channel shortening was enhanced by increasing the annealing temperature, suggesting fluorine diffusion mainly occurred during post-fabrication annealing. Since fluorine migration in an IGZO channel can be explained by hopping, the results suggest that the density of hopping site at a backchannel interface may be much larger than that in an IGZO channel [17].

6.3.4 Stabilities of BGSA IGZO TFTs

Fig. 6.6 shows the PBTS results for the BGSA IGZO TFTs with SiN_X:F-Pa at 300 °C after 1h annealing. Changes in the transfer characteristics of the BGSA IGZO TFTs with SiN_X:F-Pa were evaluated under a V_{GS} stress of +20 V with grounded V_{DS}, at stress temperatures of RT, 50, 75, and 100 °C. For the BGSA IGZO TFT with SiN_X:F-Pa, transfer curves shifted in a positive V_{GS} direction without S degradation of 1.19 V after PBTS of 10^4 s at RT, as shown in Fig. 6.6(a). The stress temperature dependence of V_{th} shift is shown in Fig. 6.6(b). The positive V_{th} shift increased with stress temperature; in addition transfer curves of the TFTs with SiN_X:F+-Pa shifted to a positive V_{GS} direction of 3.21 V with no definite change in S after PBTS of 10^4 s at 100 °C. Free electrons were trapped at the GI/IGZO interface, which induced the positive V_{th} shift.

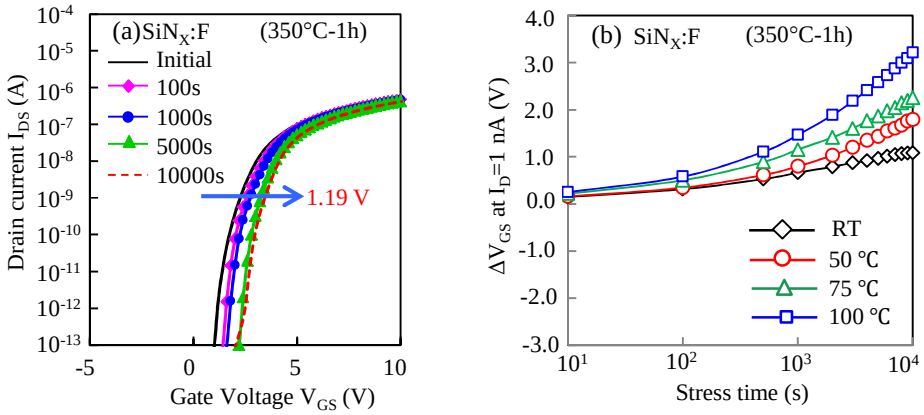

Fig. 6.6 (a) Change in transfer characteristics during PBTS at RT for the BGSA IGZO TFTs with SiN_X:F passivations after N_2 annealing at 300 °C for 1h. (b) Threshold voltage

shift (ΔV_{th}) profiles of the TFTs with SiN_X:F passivation as a function of stress time under stress temperatures of RT, 50, 75, and 100 °C.

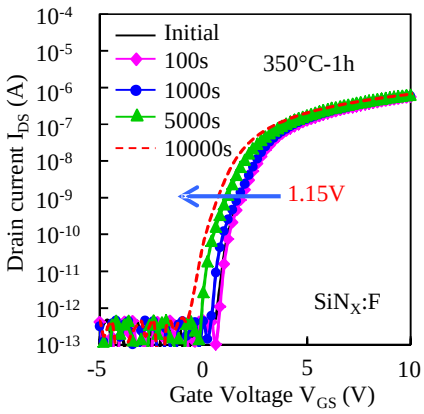

Fig. 6.7 Change in transfer characteristics during NBS without light for the BGSA IGZO TFTs with SiN_X:F passivations after N_2 annealing at 300 °C for 1h.

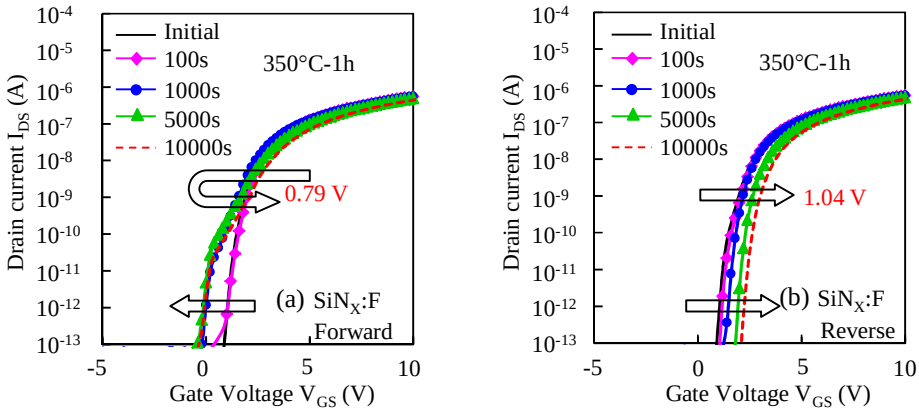

Fig. 6.8 Change in transfer characteristics during NBIS (λ=460 nm) for the BGSA IGZO TFTs with SiN_X:F passivations after N_2 annealing at 300 °C for 1h by a double sweeping V_{GS} mode. Summarized transfer curves in (a) forward and (b) reverse measurements obtained from a double sweeping V_{GS} mode.

Changes in the transfer characteristics of the BGSA IGZO TFTs with SiN_X:F-Pa were evaluated under a V_{GS} stress of -20 V with grounded V_{DS} at stress temperatures of RT with or without blue light (wavelength of 460 nm). Fig. 6.7 shows the NBS results

without light illumination for the BGSA IGZO TFTs with SiN_X:F-Pa. Transfer curves shifted to a negative V_{GS} direction of 1.15 V during NBS of 10^4 s at RT. Then, when we added light illumination, on-current degradation in forward measurement and positively parallel shift in reverse measurement were also observed for the BGSA IGZO TFT with SiN_X:F-Pa under NBIS as shown in Fig. 6.8. NBIS degradation mechanism of the BGSA IGZO TFT with SiN_X:F-Pa was already described in detail in chapter 4.

The CCS stability of BGSA IGZO TFTs with SiN_X:F-Pa was also investigated. Figure 6.9 showed the variation in the transfer characteristics with CCS duration at a current of 120 μA at RT and 50 °C for the BGSA IGZO TFTs with SiN_X:F-Pa. Transfer curves shifted 0.62 and 0.85 V after CCS of 10^4 s at RT and 50 °C, as shown in Fig. 6.9(a) and 6.9(b), respectively.

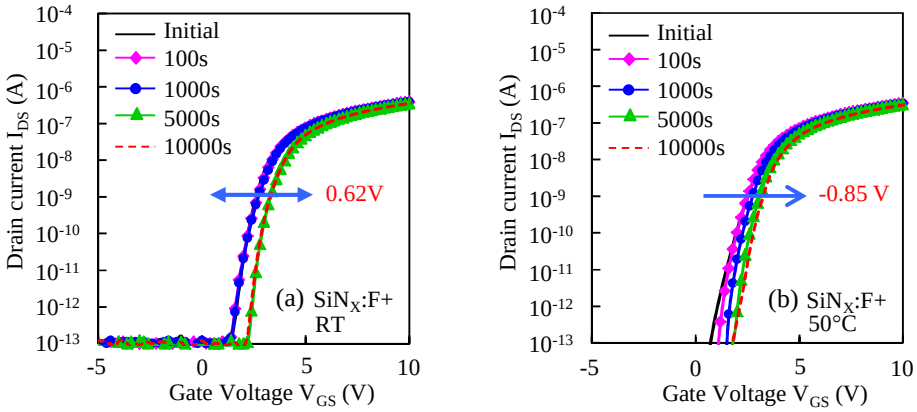

Fig. 6.9 Change in transfer characteristics during CCS for the BGSA IGZO TFTs with SiN_X:F passivations after N_2 annealing at 300 °C for 3h at (a) RT, (b) 50 °C.

The stabilities of the BGSA IGZO TFT with SiN_X:F-Pa after 1h annealing under PBTS, NBIS and CCS were also investigated. The electrical properties and stabilities of BGSA IGZO TFTs with SiN_X:F passivation was comparable to that of bottom-gate with an etch-stopper IGZO TFTs with SiO_X passivation at 350 °C after 1h annealing.

6.4 Conclusions

We proposed a novel method for making a thermally stable IGZO homojunction formed by the selective deposition of SiN_X:F on top of the IGZO. The resistivity of

IGZO/SiN_X:F stack for the S/D regions of the TFT was highly stable after annealing, and it obtained 4.1 × 10^{-3} Ωcm after N_2 annealing at 350 °C (resistivity of as-fabricated IGZO/SiN_X:F stack was 3.3×10^{-3} Ωcm.). By combining the back-side-exposure technique and IGZO homojunction formed by the direct deposition of SiN_X:F on the IGZO, a bottom-gate and self-aligned IGZO TFT was demonstrated. As a result of the thermally stable resistivity of IGZO/SiN_X:F stack for the source and drain (S/D) regions of the TFT, the TFT properties with the IGZO/SiN_X:F in the S/D regions were drastically improved compared with those of IGZO/SiO_X in the S/D regions. A field effect mobility of 10.6 $cm^2V^{-1}s^{-1}$ and an ON/OFF current ratio of over 10^8, with width-normalized $R_{S/D}$ ($R_{S/D}$W) of 33 Ωcm and the Δ*L* of 1.3 μm, were obtained after 300 °C annealing. The stabilities of BGSA IGZO TFTs were also investigated at different bias stress with or without illumination. The electrical property and stabilities of BGSA IGZO TFTs with SiN_X:F passivation at 300 °C after 1h annealing was comparable to that of bottom-gate with an etch-stopper IGZO TFTs with SiO_X passivation at 350 °C after 1h annealing. Further improvement of stabilities is required for the BGSA IGZO TFTs with SiN_X:F-Pa. Based on the findings of chapter 4. It is strongly recommended to consider long time annealing method.

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Chapter 7
Summary

Physical models to analyze the influence of defects on electrical properties were set up using device simulation. In addition, my research studied the influence of DOS in In-X-Zn-O (X=Sn, Ga) semiconductor on electrical properties of TFTs. To improve performance and stabilities for oxide TFTs, reduction and/or passivation of DOS method were investigated. I proposed a novel F passivation method of oxygen deficiencies and/or weakly bonded oxygen in oxide semiconductors using SiN_X:F as a fluorine source. The electrical and chemical properties of SiN_X:F/IGZO stacked layers were analyzed. It was found that F drastically terminated oxygen vacancies in IGZO after annealing. However, F substituted M-O to M-F bond and generated carries in IGZO simultaneously. To control F content in an IGZO channel, we proposed a novel F doping concept. Etch-stopper of SiO_X that was formed between IGZO channel and SiN_X:F passivation layer was used to control the F concentration in the IGZO channel. Highly stable fluorine-passivated IGZO TFTs were developed through long time annealing. Advanced optimization of fabrication parameters of F concentration in SiN_X:F passivation were further discussed. We successfully achieved high performance fluorine-passivated IGZO TFTs by reducing the annealing time through increasing the F concentration in SiN_X:F passivation layer. On the other hand, the resistivity and its thermal stability of IGZO/SiN_X:F stacks for applying the S/D region of the TFT were evaluated. Thermally stable $\rho_{S/D}$ was achieved by direct deposition of SiN_X:F on top of the IGZO, indicating that the IGZO/SiN_X:F stacks are very suitable for applying S/D regions of the IGZO TFTs. By combining the back-side-exposure technique and IGZO homojunction formed by the direct deposition of SiN_X:F on the IGZO, a BGSA IGZO TFT was demonstrated. The main conclusions of this thesis are summarized as follows:

I. Study of the effects of density of states in In-X-Zn-O (X=Ga, Sn) on electrical performance of the TFT using device simulation

The DOS models of In-X-Zn-O (X=Sn, Ga) TFTs were set up using device simulation. The influence of DOS on electrical properties of bottom-gate amorphous InSnZnO (a-

ITZO) and IGZO TFTs were studied.

1) Superior performances of bottom-gate a-ITZO TFTs were observed, in particular steep *S* and high mobility, as compared with bottom-gate a-IGZO TFTs. The tendency for the *S* of a-ITZO TFTs to increase with decreasing T_{ITZO} was examined using two degradation mechanisms. One mechanism is the higher density of localized acceptor-like tail states in thinner a-ITZO film. The other is a stronger influence of the localized interface traps due to the decrease of channel thickness.
2) The difference between the influence of front- and back-channel interface traps on *S* and V_{on} of a-ITZO TFTs was further analyzed by means of device simulation. It was found that *S* degraded and V_{on} positive shifted when N_{af} or N_{abk} increased. Influence of N_{af} was stronger than that of N_{abk}; however, thickness dependence of variation of *S* and V_{on} showed different tendency when N_{af} and N_{abk} varied. The influence of N_{af} on *S* was independent of T_{ITZO}; furthermore, variations of N_{af} on *S* and V_{on} were hardly dependent on T_{ITZO} when N_{af} increased or decreased by 1×10^{11} $cm^{-2}eV^{-1}$. On the other hand, the influence of N_{abk} on *S* and V_{on} became significant when T_{ITZO} decreased.
3) Variations of *S* and V_{on} became larger for thinner T_{ITZO} TFT when N_{abk} increased or decreased by 1×10^{11} $cm^{-2}eV^{-1}$; these phenomena can be explained by the screening length. The screening length is estimated to be in the range of 78-81 nm. When channel thickness is thinner than the screening length, back-channel interface traps caused deterioration in *S* and a positive shift of V_{on}, especially for thinner ITZO TFT. When channel thickness exceeds the screening length, back-channel interface traps have almost no effect on the subthreshold swing value.
4) Simulation results confirmed that not only N_{af} but also N_{abk} are important factors of *S* and V_{on} for thinner channel TFTs in work to achieve high performance oxide TFTs. The proposed thickness-dependent analysis method for front- and back-channel interface traps could become a useful tool for optimization of the fabrication process of oxide TFTs.

II. Highly stable fluorine-passivated IGZO TFTs through long time annealing

The electrical properties and stabilities of IGZO TFTs with SiO_X and SiN_X:F passivation were investigated after 1h and 3h annealing. Highly stable fluorine-passivated

IGZO TFT was developed through long time annealing. More significant improvements in the performance and stabilities of IGZO TFTs were achieved by SiN_X:F passivation as compared with SiO_X passivation after 3h annealing.

1) For the TFT with SiO_X-Pa, μ, S, and hysteresis remained almost unchanged as the annealing time increased from 1 to 3h. However, V_{th} shifted from 2.30 to 1.67 V when the annealing time increased from 1 to 3h. On the other hand, the IGZO TFT with SiN_X:F-Pa showed a higher μ, a steeper S, and a smaller hysteresis than the TFT with SiO_X-Pa even after annealing for 1h. It is interesting to note that the improvements of S and hysteresis were confirmed for the TFT with SiN_X:F-Pa as the annealing time increased to 3h. The V_{th} of the TFT with SiN_X:F-Pa shifted from 1.31 to -0.37 V when the annealing time increased from 1 to 3h.
2) No difference in H (m/z=1) content was observed in either the ES-SiO_X or IGZO between the SiN_X:F-Pa and SiO_X-Pa samples. H (m/z=1) profile remained almost unchanged in the IGZO layer as the annealing time increased from 1 to 3h. However, a large difference in m/z=19 content in the SiO_X-ES layers was observed between the SiO_X-Pa and SiN_X:F-Pa samples even after 1h annealing. The large difference in m/z=19 content in the SiO_X-ES layer with SiN_X:F-Pa results from fluorine. When the annealing time increased to 3h, an increase in m/z=19 content in the IGZO layer with SiN_X:F-Pa was detected. Those results indicate that the long annealing time enhanced F diffusion from the SiO_X-ES layer to the IGZO channel when F existed in the SiO_X-ES layer.
3) The ΔV_{th} under PBTS with a V_{GS} stress of +20 V for 10^4 s was markedly reduced from -6.24 V for the TFT with SiO_X passivation to -0.45 V for the fluorine-passivated IGZO TFT (TFT with SiN_X:F passivation after 3h annealing) even at a stress temperature of 100 °C. NBIS degradation phenomena of IGZO TFT with SiO_X-Pa were effectively suppressed by fluorine-passivated IGZO TFT, forward and reverse transfer curves shifted 0.33 V and 0.19 V, respectively, even at the NBIS time of 10^4 s. Hysteresis V_H of transfer curves under NBIS with V_{GS} stress of -20 V for 10^4 s was drastically reduced from 4.31 V for the TFT with SiO_X passivation to 0.16 V for the fluorine-passivated IGZO TFT at a wavelength of 460 nm. Furthermore, the fluorine-passivated IGZO TFTs also had high stability under CCS; transfer curves shifted to a

negative V_{GS} direction of 0.07 and 0.43 V after CCS of 10^4 s at RT and 50 °C, respectively.

4) SIMS analysis revealed that stabilities of the IGZO TFT with SiN_X:F passivation were markedly improved when the diffusion of F into the IGZO channel from a SiO_X etching stopper (SiO_X-ES) was confirmed after post-fabrication annealing. We found that diffused F effectively passivated oxygen vacancies and weakly bonded oxygen in the IGZO channel and at the GI/channel interface, resulting in improved performance and stabilities of IGZO TFTs including PBTS, NBIS and CCS stabilities. The proposed method of fluorinating IGZO TFTs is suitable for application in next generation FPD.

III. Highly stable F+ passivated IGZO TFTs

Advanced optimization of fabrication parameters of F concentration in SiN_X:F passivation were further discussed. The electrical property and stability of IGZO-TFT with SiN_X:F+ passivation were investigated.

1) The IGZO TFT with SiN_X:F+ passivation showed steep subthrehold swing (<0.20) and small hysteresis (<0.10), which can be compared with that of IGZO TFTs with SiN_X:F passivation after 3h annealing. In addition, V_{th} of IGZO TFT with SiN_X:F+ passivation shifted in a positive V_{GS} direction by about 1 V as compared with IGZO TFTs with SiN_X:F passivation after 3h annealing.

2) The positive V_{th} shift increased with stress temperature; finally, transfer curves of the TFTs with SiN_X:F+-Pa shifted in a positive V_{GS} direction of 0.87 V with no definite change in S after PBTS of 10^4 s at 100 °C. NBIS degradation phenomena of IGZO TFT with SiO_X-Pa were also effectively suppressed by SiN_X:F+-Pa, Forward and reverse transfer curves shifted 0.28 V and 0.28 V, respectively, even at the NBIS time of 10^4 s; Hysteresis V_H shift was dramatically reduced to 0.12 V after NBIS time of 10^4 s. For the TFT with SiN_X:F+-Pa, transfer curves shifted to a negative V_{GS} direction of 0.12 and 0.5 V, respectively, after CCS of 10^4 s at RT and 50 °C. We also achieved good uniformity in short-range region for the TFTs with SiN_X:F+-Pa. The electrical properties and stabilities of IGZO-TFT with SiN_X:F+ passivation after 1h annealing is comparable to that of IGZO TFTs with SiN_X:F passivation after 3h annealing.

3) F (m/z=19) profile larger in SiO_X-ES for without annealing TFTs with SiN_X:F+-Pa as compared with that of SiN_X:F-Pa TFTs indicating that 1hour annealing is enough for F diffusion from the SiO_X-ES layer to the IGZO channel, if larger F existed in the SiO_X-ES layer. The highly stable F+ passivated IGZO TFT has good stabilities and uniformity, and is advantageous for application in next-generation displays.

IV Self-aligned bottom-gate In-Ga-Zn-O thin-film transistor with source/drain regions formed by direct deposition of fluorinated silicon nitride

We proposed a novel method for making a thermally stable IGZO homojunction with highly conductive region that was selectively formed by a direct deposition of SiN_X:F on top of the IGZO film. By combining the back-side-exposure technique and IGZO homojunction formed by the direct deposition of SiN_X:F on the IGZO, a BGSA IGZO TFT was demonstrated. The stabilities of BGSA IGZO TFTs were also investigated at different bias stress with or without illumination.

1) For the IGZO/SiO_X stack, $\rho_{S/D}$ was 1.9×10^{-2} Ωcm before annealing. However, recovery of the $\rho_{S/D}$ was observed after N_2 annealing at 250 °C, and the $\rho_{S/D}$ increased to over $2\times10^{+8}$ Ωcm as the annealing temperature increased to 300 °C. On the other hand, $\rho_{S/D}$ of as-fabricated IGZO/SiN_X:F stack was 3.3×10^{-3} Ωcm. The resistivity of IGZO/SiN_X:F stack for the S/D regions of the TFT was highly stable after annealing, and it obtained 4.2×10^{-3} Ωcm after N_2 annealing at 300 °C.
2) As a result of thermally stable resistivity of IGZO/SiN_X:F stack for the source and drain (S/D) regions of the TFT, the TFT properties with the IGZO/SiN_X:F in the S/D regions improved drastically compared with those of IGZO/SiO_X in the S/D regions. Field effect mobility of 10.6 $cm^2V^{-1}s^{-1}$ and an ON/OFF current ratio of over 10^8 were obtained after 300 °C annealing.
3) The width-normalized $R_{S/D}$ ($R_{S/D}$W) of 33 Ωcm and ΔL of 1.3 μm was obtained for BGSA IGZO TFTs after 300 °C annealing. Channel shortening was enhanced as increasing annealing temperature, suggesting fluorine diffusion mainly occurred during the post-fabrication annealing.
4) The positive V_{th} shift increased with stress temperature and, finally, transfer curves of the BGSA IGZO TFTs with SiN_X:F-Pa shifted in a positive V_{GS} direction of 3.21 V

with no definite change in *S* after PBTS of 10^4 s at 100 °C. On-current degradation in forward measurement and positively parallel shift in reverse measurement were also observed for the BGSA IGZO TFT with SiN_X:F-Pa under NBIS. Transfer curves shifted about 0.62 and 0.85 V after CCS of 10^4 s at RT and 50 °C. The proposed method is therefore essential for making self-aligned oxide TFTs with thermally stable S/D regions.

As a consequence, we proposed a thickness-dependent analysis method, a novel F passivation IGZO method, and a novel self-align structure with thermally stable S/D regions in order to develop high performance and stability oxide TFTs for future electric device applications.

Appendix: Publications and presentations resulting from the thesis

Published Journal:

[1] **J. Jiang**, M. Furuta, and D. Wang, "Self-aligned bottom-gate In-Ga-Zn-O thin-film transistor with source/drain regions formed by direct deposition of fluorinated silicon nitride," IEEE Elec. Dev. Lett. Vol. 35, No. 9, pp. 933-935, (2014).

[2] **J. Jiang**, T. Toda, M. P. Hung, D. Wang and M. Furuta, "Highly Stable Fluorine Passivated In-Ga-Zn-O Thin-Film Transistors under Positive Gate Bias and Temperature Stress," Appl. Phys. Express, Vol. 7, pp. 114103, (2014).

[3] **J. Jiang**, T. Toda, G. Tatsuoka, D. Wang and M. Furuta, "Improvement of Electrical Properties and Bias Stability of Ingazno Thin-Film Transistors By Fluorinated Silicon Nitride Passivation," ECS Trans. Vol. 64, No. 10, pp. 59-64, (2014).

[4] **J. Jiang**, D. Wang, T. Matsuda, M. Kimura, and M. Furuta, "Influence of Front- and Back-Channel Interface Traps on Electrical Properties of Oxide TFTs with Different Channel Thicknesses," (Ready to submit).

[5] T. Toda, D. Wang, **J. Jiang**, M. P. Hung, and M. Furuta, "Quantitative Analysis of the Effect of Hydrogen Diffusion from Silicon Oxide Etch-Stopper Layer into Amorphous In–Ga–Zn–O on Thin-Film Transistor," IEEE trans. Electr. Dev. Vol. 61, No. 11, pp. 3762-3767, (2014).

[6] D. Wang, M. P. Hung, **J. Jiang**, T. Toda, C. Li, M. Furuta, "Effect of Drain Bias on Negative Gate Bias and Illumination Stress Induced Degradation in Amorphous InGaZnO Thin-Film Transistors", Jpn. J. Appl. Phys. Vol. 53, pp. 03CC01-1-03CC01-4 (2014).

[7] D. Wang, M. P. Hung, **J. Jiang**, T. Toda, and M. Furuta, "Suppression of degradation induced by negative gate bias and illumination stress in amorphous InGaZnO thin-film transistors by applying negative drain bias", ACS Appl. Mater. Interfaces, Vol. 6, No. 8, pp. 5713-5718 (2014).

[8] M. Furuta, **J. Jiang**, G. Tatsuoka, and D. Wang, "Self-Aligned Bottom-Gate InGaZnO Thin-Film Transistor with Source and Drain Regions Formed by Selective Deposition of Fluorinated SiNx Passivation", ECS Trans. Vol. 64, No. 10, pp. 53-58, (2014).

[9] D. Wang, M. P. Hung, **J. Jiang**, T. Toda, and M. Furuta, "Drain Bias Effect on the Instability of Amorphous InGaZnO Thin-Film Transistors under Negative Gate Bias and Illumination Stress", ECS Trans. Vol. 64, No. 10, pp. 65-70, (2014).

[10] M. P. Hung, D. Wang, **J. Jiang**, and M. Furuta, "Negative Bias and Illumination Stress Induced Electron Trapping at Back-Channel Interface of InGaZnO Thin-Film Transistor", ECS Solid State Lett. Vol. 3, No. 3, pp. Q13-Q16, (2014).

[11] M. P. Hung, D. Wang, T. Toda, **J. Jiang**, and M. Furuta, "Quantitative Analysis of Hole-Trapping and Defect-Creation in InGaZnO Thin-Film Transistor under Negative-Bias and Illumination-Stress", ECS J. Solid State Sci. and Tech. Vol. 3, No. 9, pp. Q3023-Q3026, (2014).

[12] M. Furuta, M. P. Hung, **J. Jiang**, D. Wang, S. Tomai, H. Hayasaka, and K. Yano, "Negative-Bias with Illumination Stress Induced State Creation in Amorphous InGaZnO Thin-Film Transistor", ECS Trans. Vol. 54, No. 1, 127-134, (2013).

[13] T. Matsuda, M. kimura, **J. Jiang**, D. wang, M. Furuta, and M. Kasami, "Trap States in Amorphous In-Sn-Zn-O Thin-Film Transistors Analyzed Using Dependence on Channel Thickness", SID Symposium Digest of Technical Papers, Vol. 44, No. 1, 1014-1017, (2013).

International conference:

1. Extraction of trap density on oxide thin-film transistors with various channel thickness (Oral, 4C-Oxide2, pp. 335-336), **Jingxin Jiang**, Dapeng Wang, Chaoyang Li and Mamoru Furuta. The Twentieth Annual International Conference on Composite/Nano Engineering (ICCE-20), July 22-28, 2012. Beijing, China.
2. Influence of Front- and Back-Channel Interface Traps on Electrical Properties of Oxide TFTs with Various Channel Thicknesses (Poster, 1pLP42, pp. 76). **Jingxin Jiang**, Dapeng Wang, Mutsumi Kimura, and Mamoru Furuta. International Thin-Film Transistor Conference in 2013 (ITC). Mar. 1-3, 2013. Tokyo, Japan.
3. Interface Traps Influence on the Properties of InSnZnO Thin-Film Transistors with Different Channel Thicknesses (Oral). **Jingxin Jiang**, Dapeng Wang, Tokiyoshi Matsuda, Mutsumi Kimura, and Mamoru Furuta. The 3rd International Symposium on Frontier Technology (ISFT). July 26-29, 2013. Shenyang, China.

4. Improvement of electrical properties of InGaZnO thin-film transistors by fluorinated silicon nitride passivation (Oral). **Jingxin Jiang**, Toda Tatsuya, and Mamoru Furuta. The Japan Society of Applied Physics. March 17-20, 2014. Japan.
5. Improvement of Electrical Properties and Bias Stability of InGaZnO Thin-Film Transistors by Fluorinated Silicon Nitride Passivation (Oral). **Jingxin Jiang**, Toda Tatsuya, G. Tatsuoka, and Mamoru Furuta. 2014 ECS and SMEQ Joint International Meeting. October 6-9, 2014. Mexico.
6. Improvement of Positive Bias and Temperature Stress stability by Fluorine Passivated In-Ga-Zn-O Thin-Film Transistors (Oral). **Jingxin Jiang**, Toda Tatsuya, Dapeng Wang, and Mamoru Furuta. The 21st International Display Workshops. December 3-5, 2014, Japan.

Awards:

I received the Best Student Poster Presentation Award at International Thin-Film Transistor Conference in 2013 (ITC'13).