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Master's thesis

A Programmable Cycle-by-Cycle Dynamic Clock Adjustment and its FPGA Implementation with RISC-V Core

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Abstract

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This dissertation presents a programmable cycle-by-cycle dynamic clock adjustment (PDCA) into the next level of profile-based with dynamically varying program execution by using average clock frequency. That could be applied to any micro-architecture such as MIPS, OpenRISC, RISC-V and ARM as intellectual property core. An architecture allows users to decide the operation mode flexibly using software control. That made PDCA has no limitation by the worst-case execution time and micro-architecture functionality. The performance evaluation has been demonstrated in term of power consumption reduction by 25 % and throughput improvement up to 40 % The proposed architecture offers a potential alternative to low power design for green data warehouse, internet of things processors, and complex mathematic solver machine.

key words RISC-V, Low-power, Programmable Cycle-by-Cycle Dynamic Clock Adjustment, Profile-based frequency scaling, Time-Average-Frequency.